Patent Title:

OFFH-CDM ALL-OPTICAL NETWORK

Inventor:
FOULI K., MENIF M., LADDADA R., AND **FATHALLAH H**.

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OFFH-CDM ALL-OPTICAL NETWORK

FIELD OF THE INVENTION

The present invention relates to the filed of optical networking architectures. More particularly, it relates to the establishment of all-optical communication between OFFH-CDM transmitters and receivers through a generalized optical-fiber mesh network.

BACKGROUND OF THE INVENTION

The last decade has witnessed a steady increase in telecommunication applications that require high-bandwidth connections to be established fast, over various optical fibre physical topologies, and between an increasing number of connected terminals. Networking architectures that provide complete and feasible solutions are therefore required.

In the field of optical communications, several architectures have been proposed to connect transmitters and receivers. Photonic networks have been proposed that use single-wavelength or waveband WDM circuit connections between network terminals. Packet-switched architectures that use single-wavelength WDM labels to route packets to an appropriate destination have also been proposed.

In a projected network architecture described in a US patent (H. Fathallah et al., "Fast frequency hopping spread spectrum for code division multiple access communications networks," U.S. no. 6,381,053, 4/2002) time and wavelength (spectro-temporal codes) are used to encode information in such a way that only the recipient with the proper decoder can retrieve the information, which was broadcasted to all the receiving terminals in the network.

In a preferred implementation of an OFFH-CDM transmitter, an optical pulse from a broadband source is sliced in many wavelength bands (or wavebands), each one being delayed relative to the other in such a way that an optical code is generated, using a series of fibre Bragg gratings.

The reference patent covers transmission and reception of OFFH-CDM signals in a single broadcast medium. To support large networks, it is important to move from a broadcast to a switched system, thus removing the addressing limit of the single OFFH-CDM medium in terms of the total number of users (or terminals). This creates a physical layer based on OFFH-CDM that can be implemented at various network levels: not only the local area but also at metropolitan-area network (MAN) and wide-are network (WAN) levels.

Moving to a switched environment provides support for more general physical topologies such as mesh networks. In addition, a switched architecture is more likely to handle various higher level traffic protocols such as the Internet Protocol (IP), Asynchronous Transfer Mode (ATM), Multi-Protocol Label Switching (MPLS) in a straightforward manner.

SUMMARY OF THE INVENTION

The present invention proposes two distinct architectures for designing all-optical mesh networks using Optical Fast-Frequency Hop Code Division Multiplexing technology. The first architecture is circuit-switched and is based on assigning different codes to different circuits for each network leg. The second architecture is packed-switched and relies on duplicating and filtering packets using a novel addressing scheme and routing technique.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 Definition of the all-optical domain, the design requirement.

FIG. 2 (A) Circuit-switched network design showing a circuit connection between two distant ports that utilizes 3 different codes for its 3 legs (hops). (B and C) Two alternative router node switching architectures.

FIG. 3 The functional equivalence of encoder/decoder tunability and switching prior to the encoding/decoding stage.

FIG. 4 (A and B) Two alternative edge node architectures.

FIG. 5 Conversion module (CM) block diagram (A), and two alternative implementations (B and C).

FIG. 6 (a) Packet Routing (b) router with packet gate architecture.

FIG. 7 (a) Addressing space and (b) Packet Format.

FIG. 8 Fixed-duration Packet Gate.

FIG. 9 Fixed-duration Packet Gate Implementation.

FIG. 10 Variable-duration Packet Gate.

FIG. 11 Variable-duration Packet Gate Implementation.

FIG. 12 All-optical Packet Router Based on Tunable Gate Arrays.

FIG. 13 All-optical Packet Router Based on Fixed Gate Arrays.

FIG. 14 Block Diagram for OCDM Packet Transmitter.

FIG. 15 Transmitter Configuration with Header/Footer Implementation.

FIG. 16 Transmitter Configuration with Modulator/ Switch.

FIG. 17 Edge-Node for Packet-Switched Network.

FIG. 18 3-Level Addressing Space and Packet Format.

FIG. 19 Photonic Label Swapping (Fixed packet duration).

FIG. 20 Photonic Label Swapping (Variable packet duration).

FIG. 21 All-optical CDM Packet Encapsulation.

DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Generally, the present invention relates to a method and system for testing an optical network for defects between a network node and a plurality of network locations.

All-optical routing is the essential technology enabler for optical metropolitan and backbone networks. The final aim of most current designs is to remove electronics from core networks completely. That

implies inter-connecting electronic ports at different edge nodes (ENs) optically through EN transceivers and all-optical router nodes (see FIG. 1), where edge nodes are electronic-to-optic (E/O) access nodes.

In a circuit-switched network, ports represent the interface of individual electronic high-capacity connections such as SONET optical carriers (OC), or native ATM virtual paths (VP), with the optical core network. Circuit-switched basic requirements include the ability to set-up transparent and reconfigurable connections between any transceiver pair all-optically.

Ports in a packet-switched scenario are the interfaces of electronic packet sources such as IP routers. An all-optical packet-switched network requires the development of fast routing mechanisms and a global addressing scheme.

A. Circuit-Switched Solution

Each routing node (RN) links at least one input leg to one output leg. Each network leg carries at least one fiber.

In this invention, circuits are set-up by network management. Port receivers are fixed OFFH-CDM decoders, distinct at each EN. A circuit set from one port to another may use a different code over each leg. Routing nodes switch the corresponding connections together all-optically, and require the all-optical conversion of data from one code to another. These concepts are illustrated in FIG. 2 A, where two edge-node ports are connected by a 3-leg circuit using a different code on each leg.

The basic router node switching architecture is depicted in FIG. 2 B. Power from each input fiber is split among an array of decoders that represent all available codes on all input legs. A conversion module (CM) transforms decoded data pulses into broadband pulses optically. Such a device is discussed below.

At the next stage, a space-switch directs encoded power to the corresponding output fiber. Before entering the fiber, data is encoded at one of the codes used in that fiber. Many variations of this design may ensure identical functionality. One major variation is shown in FIG. 2 C. In this design, the positions of the switching and encoding stages are interchanged. In addition, encoding is tunable (assigned codes are dynamic) and managed by network control. First, each tunable encoder is adjusted to the required code for the next leg, and then encoded data is switched to the required fiber. This method allows network control to insure the dynamic reusability of codes on different output fibers. If all output codes are distinct, it is possible to replace the switch by a splitter-combiner. Besides, tunability may be implemented at the decoding stage rather than the encoding stage. If the set of codes associated to each link is required to be a dynamic set, both the decoding and the encoding stages need to be tunable.

At any encoding or decoding stage, tunability may be removed without loss of functionality by using an additional switch at the input of an array of fixed encoders/decoders, as shown in FIG. 3.

It should be noted that legs are not necessarily unidirectional. The use of circulators to connect router-node input and output fibers to leg-fiber avoids eventual coupling loss.

Edge nodes perform two major functionalities: add-drop of electrical circuits, and all-optical routing. FIG. 4 depicts two equivalent EN architectures. In FIG. 4 A, ports setting off circuits on the network are labeled “Electronic Add”. Electrical-to-Optical interfaces (E/O) convert electrical signals to broadband data pulses ready for OFFH-CDM encoding and transmission. The encoders in FIG. 4 A may be fixed rather than tunable.

Circuits reaching the EN may be dropped at the node or switched towards other routing/edge nodes. Regardless, they are all decoded and passed through a switching stage. The circuits to be dropped are directed towards the Optical-to-Electrical interface (O/E) where they terminate at electrical ports. The circuits to further be routed go through usual conversion, encoding, and switching stages. FIG. 4 B describes a variation of the EN architecture that unifies the input and output switching stages and permits the looping of circuits back to other electrical ports of the same EN.

The circuit-switching architectures presented above enable the setting of transparent configurable circuits. QoS differentiation and multi-rate services can be supported by such an OFFH-CDM network. The use of the entire coding space (all available codes) in each fiber of each leg implies considerable granularity advantages: great numbers of low bit-rate flows may be routed without strenuous TDM processing. For instance, such network architecture supports the end-to-end processing of large numbers of SONET circuits (OC-3 or less).

FIG. 5 A depicts the intended function of a conversion module. The input consists of the realigned chip pulses that leave the optical decoder (decoder output). The required output is a single broadband pulse. The operation of transforming autocorrelation peaks to broadband pulses may or may not use internal electronics (i.e. electrical detection).

Two conversion module implementations follow. The first configuration, depicted in FIG. 5 B represents an electro-optical pulse regeneration mechanism. At the optical input, the decoded OFFH-CDM pulse activates an electrical trigger circuit (shaded and labeled “TRIGGER”). The trigger circuit in turn activates an ultra-fast optical switch for a time-duration equivalent to a chip. The delay mechanism may be implemented within the optical gate or electrically within the trigger circuit. The trigger circuit may be built such that it is insensitive below a certain threshold of input optical power in order to eliminate interference and noise.

The second proposed configuration cascades two SOAs (Semiconductor Optical Amplifiers), as shown in FIG. 5 C, in order to achieve the exact replica of the input waveform. This requires modulation depths close to unity for both SOAs. A circulator was added to prevent feedback amplification between the two SOAs. The input device (generating Pin) may be protected from reflections by using a 4-port circulator instead.

The input of the conversion module may be a CDM decoder output to be converted to another code, as in the cases above, or any WDM signal carrying digital data that is pulsed. In the case of FIG. 5 C, CDM inputs have the advantage of reducing the device wavelength dependency. At the output of a CM, a decoder or a filter may be placed for conversion of the input to CDM or WDM respectively.

B. Packet-Switched Solution

The starting point for this invention is the search for an all-optical method to separate incoming packets according to their destination Edge Node, as described in FIG. 6 (a). As in the circuit-switched case, port receivers at each EN are assumed to be fixed and distinct OFFH-CDM decoders. Within any given EN, the CDM codes of port receivers are unique; hence each code may be viewed as a local address. Therefore, the main issue is to devise a means to distinguish and switch packets according to an addressing attribute that is common to all packets destined to the same EN.

An addressing scheme that enables all-optical fast switching on a packet-basis is to be designed. It is proposed to add an EN-specific identification header to each packet. Such a mechanism triggers gates to allow packets with the appropriate header through. Incoming packet flow is split over an array of gates, with each gate filtering packets to be routed towards a predetermined router output, as shown in FIG. 6 (b).

FIG. 7 (a) depicts the spectral addressing space that is split between EN and port addresses/codes. EN addresses are mapped onto CDM codes in the same way as local addresses (port addresses) are. Separate wavelength bands are used for port and EN codes/addresses, as depicted in FIG. 7 (a).

FIG. 7 (b) shows two possible cell formats: A network utilizing fixed cell-duration uses cells containing a header and a payload. As shown by the color code in FIG. 7 (a), the payload (port data) is encoded within the spectral addressing space of the port transceivers whereas the header (EN address) is encoded within the spectral addressing space of the edge node. In the case of a network utilizing variable packet-duration, packets are delimited on both the beginning and end by EN addressing signaling. We refer to the start-signal as a header and to the end-signal by the word footer. Headers and footers may consist of one or more OFFH-CDM pulses. Guard-times may be introduced between the signaling parts and the payload part of the cells, depending on the gates' specifications.

In the case of fixed-length packets (cells) in a fixed-rate environment, EN address information is carried by a header that activates the gates corresponding to the correct destinations. Those gates remain open for a fixed amount of time corresponding to the cell duration. Gates have fixed "open state" duration and they require ultra-fast electronic timers. If packets are of variable duration due to their variable lengths or due to the use of more than one transmission rate across the network, a packet-footer is also added to trigger gate shutting (see FIG. 7 (b)). The gate block-diagrams and preferred implementations for fixed-duration and variable-duration packet cases are presented in FIG. 8 and FIG. 10 respectively. In those implementations, packet headers and footers are single bits that are encoded in the EN's OFFH-CDM address code. The duty cycle of these pulses may be larger to allow easier detection.

FIG. 8 (a) is a block diagram of a gate for the fixed-duration packet case. Input packet power is tapped and a fraction of the power is directed towards an EN address decoder. If the packet header code matches the decoder, the recombined pulse activates a fast timer circuit. That circuit is responsible for sending the ON and OFF triggers to the optical gate, thus allowing the packet to pass. A delay may be included at the gate input to compensate for the processing time of the timer circuit.

FIG. 8 (b) is a simple state diagram describing the timer logic. The decoded pulse (Dec) sets the gate in the ON state. A subsequent decoded pulse before the end of the timer delay means a new packet with the same EN address hit the gate before its closure. In that case, the timer is reset, allowing for the passage of the new packet. Upon reaching the end of the timed delay, the timer sets the gate OFF. The preferred implementation of the gate architecture in FIG. 8 (a) is presented in FIG. 9.

Tapping can be implemented using a 13dB coupler, provided enough energy is assembled in decoded pulses to start the timer circuit. Pre-amplifiers and post-amplifiers may be implemented at the gate-level or at the router level depending on the power budget. C1 represents the EN code/address for the allowed packets. A tunable decoder is proposed for network reconfigurability purposes, thus making the gate tunable. Tunability of gate decoders is optional. Among the candidate gate technologies investigated: acousto-optical, mechanical, semiconductor optical amplifier (SOA), and electro-absorption (EA), the latter is probably the fastest and most transparent gate technology available. Its response time is lower than 20ps, and the high insertion loss (around 8 dB) may be countered by an EDFA booster at the fiber leg inputs. The timer circuit response time, which is compensated by the input delay loop, may achieve response times in the order of sub-nanoseconds.

A variable packet length or bit-rate implies variable packet duration. A footer signal is required at the end of the packet to shut the gate, and uses a code that is different from the header signal. Every EN is therefore associated to two distinct and unique codes

As shown in FIG. 10 (a), tapped input packet power is split on two distinct decoders that correspond to the header code (ON code) and the footer code (OFF code). Hence, an input packet with the right ON and OFF code will result in a counter circuit being activated. As the state diagram of FIG. 10 (b) shows, the counter circuit accounts for new transiting packets by holding an ON pulse and OFF pulse count. Hence, upon receiving an ON pulse, it triggers the gate to the ON position and starts counting ON and OFF pulses. Once the number of received OFF pulses equals that of ON ones, the counter circuit triggers the gate OFF. The preferred implementation of the variable-duration packet gate is depicted in FIG. 11.

The simplest implementation of a packet router using tunable gate arrays is shown in FIG. 12. Input packets are combined then split towards all gates. Gates feeding a given router output are tuned to the different EN addresses that are reached through that output. Router control sets gate addresses.

An alternative to gate tunability is the use of an array of all possible gate configurations along with a switch as shown in FIG. 13. The argument is similar to the one presented in FIG. 3.

We now design a transmitter that generates broadband pulses that can be modulated with the appropriate signal (header, data, and optionally footer) and encoded using the appropriate code. Such a transmitter may have the configuration depicted in FIG. 14. A broadband pulsed

source (BBPS) is modulated by header, data, or footer signaling. A switch (S) directs the broadband modulated signal to the corresponding encoder (ENC). The packet components are reassembled at the transmitter output. Dashed-line additions need to be taken into consideration only in the variable packet-duration case. In this implementation, packet components may not overlap in time. Another implementation, shown in FIG. 15, allows the overlapping of header, data, and footer electronic signaling by feeding them to different modulators. The advantage of such a scheme is that packets arriving at the E/O interface need not be buffered and queued with the header and footer signals. They can instead flow directly to the data modulator while the header/footer modulators produce the required signals to wrap all incoming packets in real-time.

Two transmitter configurations enabling the generation of optical packets with headers and footers are described in figures 15 and 16. In the first (FIG. 15) a broadband pulse source (BBPS) generates pulses at the transmitter bit-rate. The wavelength bands corresponding to port and EN addresses are separated and fed to distinct modulators. The header/footer and data pulses are thus generated separately, and are encoded by the EN address encoder (Label Encoder) and the port address encoder (user encoder) respectively. Modulators need to be timed in a way that insures the alignment of the packet components in time, at the output.

The alternative implementation of FIG. 16 uses a single modulator/switch instead of two separate modulators. Tunable encoders can be replaced by an array of fixed encoders preceded by a switch, for either EN codes or port codes.

The implementation of the edge-node in case of a packet-switched network is presented in FIG. 17. As mentioned, edge nodes perform two major functionalities: add-drop of electrical packets, and all-optical packet switching. TX represents OCDM packet transmitters. Input packets destined to the EN are filtered through the EN gate and broadcast to the fixed decoders for reception and O/E conversion.

C. Multilayered OFFH-CDM Packet Network

The concept of EN addressing may be generalized beyond the two-level scheme described above to more levels. For instance, the three-level addressing space and packet format shown in FIG. 18 enable the allocation of WAN, LAN, and station addresses/codes. A 4-level addressing space can be used to map physical-layer addresses (code quadruples) to IPv4 addresses.

The same packet-routing procedure may be used to implement label-routing mechanisms, where labels attached to packets specify their path. This requires, however, the ability of swapping labels. A label-swapping block can be placed at gate outputs. A photonic implementation of label swapping is depicted in figures 19 and 20. FIG. 19 represents a label-swapping device for fixed-duration packets. The decoded label pulse is re-encoded to the required new label code using a tunable encoder, while the packet payload is extracted with a filter, and undergoes the corresponding delay. Label and payload recombine in the correct time-order using a WDM band combiner. FIG. 20 depicts a label-swapping device for variable-duration packets. The generation of new headers and footers is triggered by the old headers and footers respectively.

It might be necessary in a packet-switched network to encapsulate packets in additional layers of headers or header/footer pairs. FIG. 21 describes an appropriate mechanism. Input packet power is tapped and used to trigger the synchronous generation of new encapsulating headers and footers. Delays in the order of bits are required. Ideally, for the packet format shown, D1 represents the sum of the processing-time delay and one bit-duration (i.e. header/footer code conversion time), whereas D2 represents a single bit duration.

Of course, numerous modifications could be made to the embodiments above without departing from the scope of the present invention.

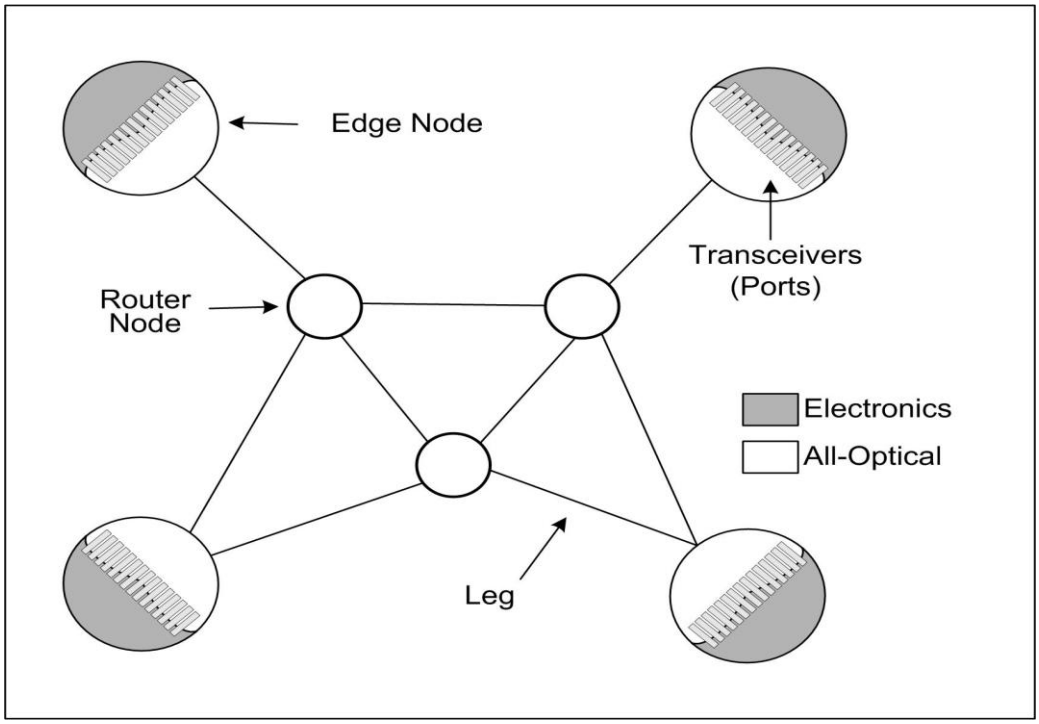

FIG. 1 Definition of the all-optical domain, the design requirement

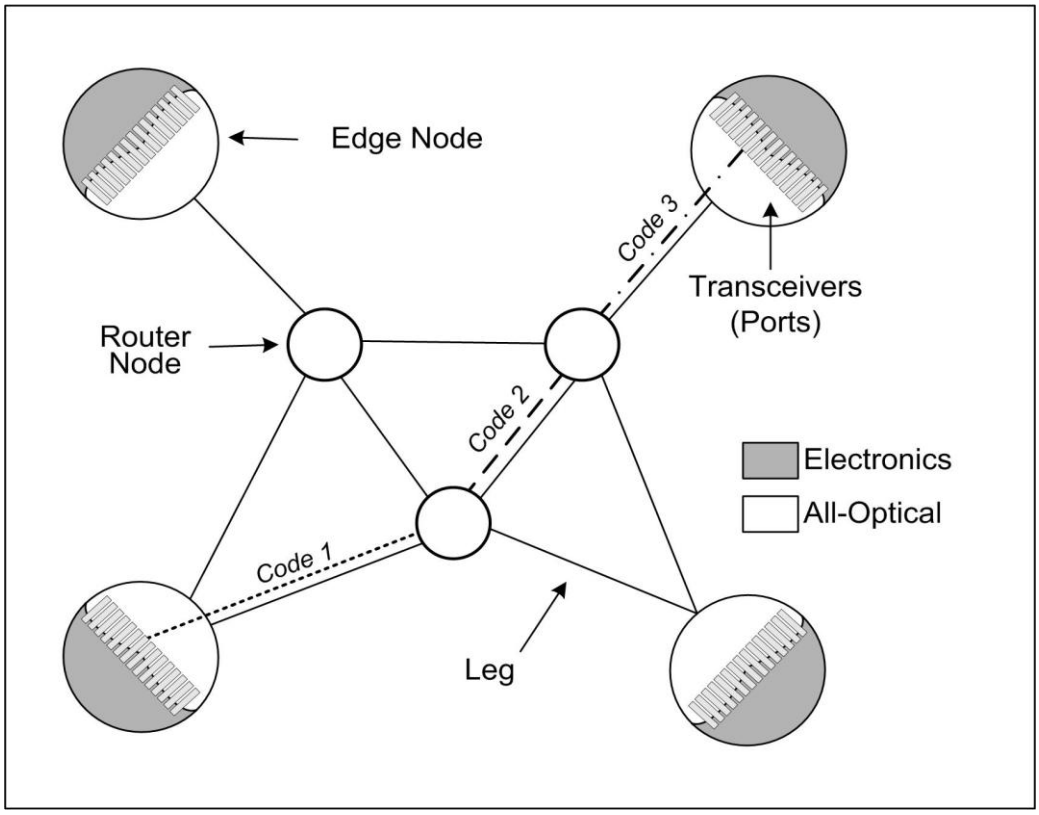

FIG. 2 (A) Circuit-switched network design showing a circuit connection between two distant ports that utilizes 3 different codes for its 3 legs (hops)

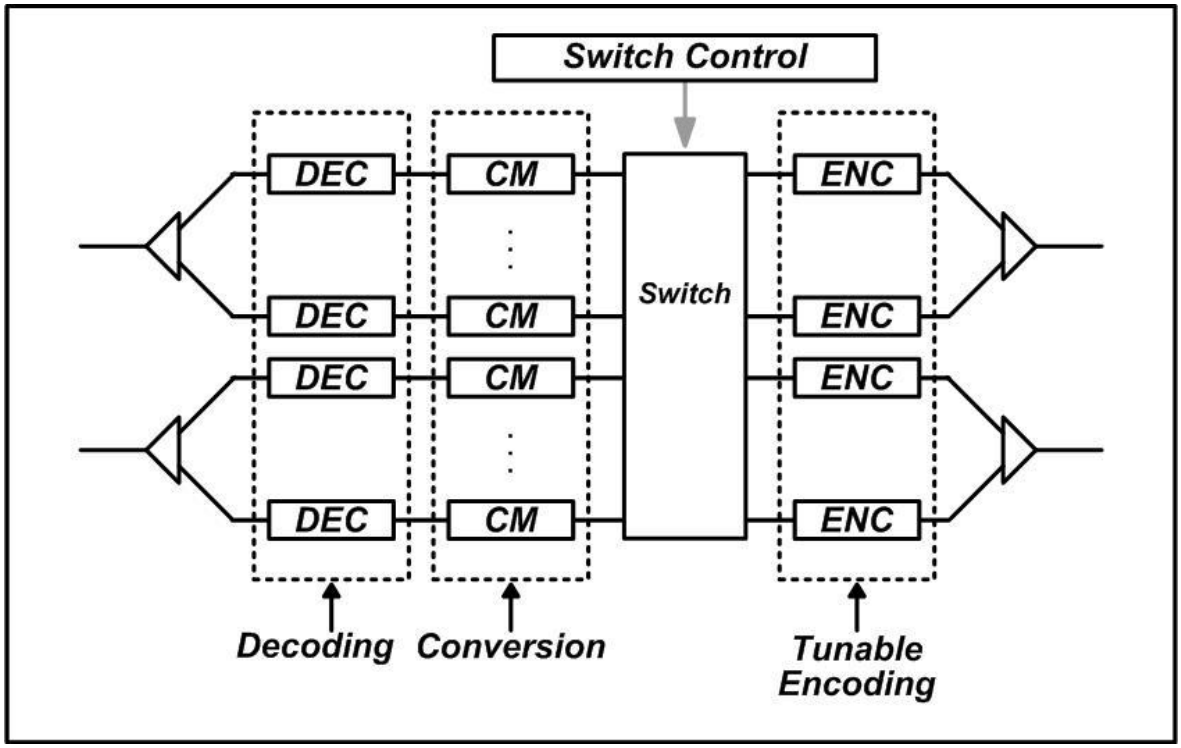

FIG. 2 (B) Router node switching architecture

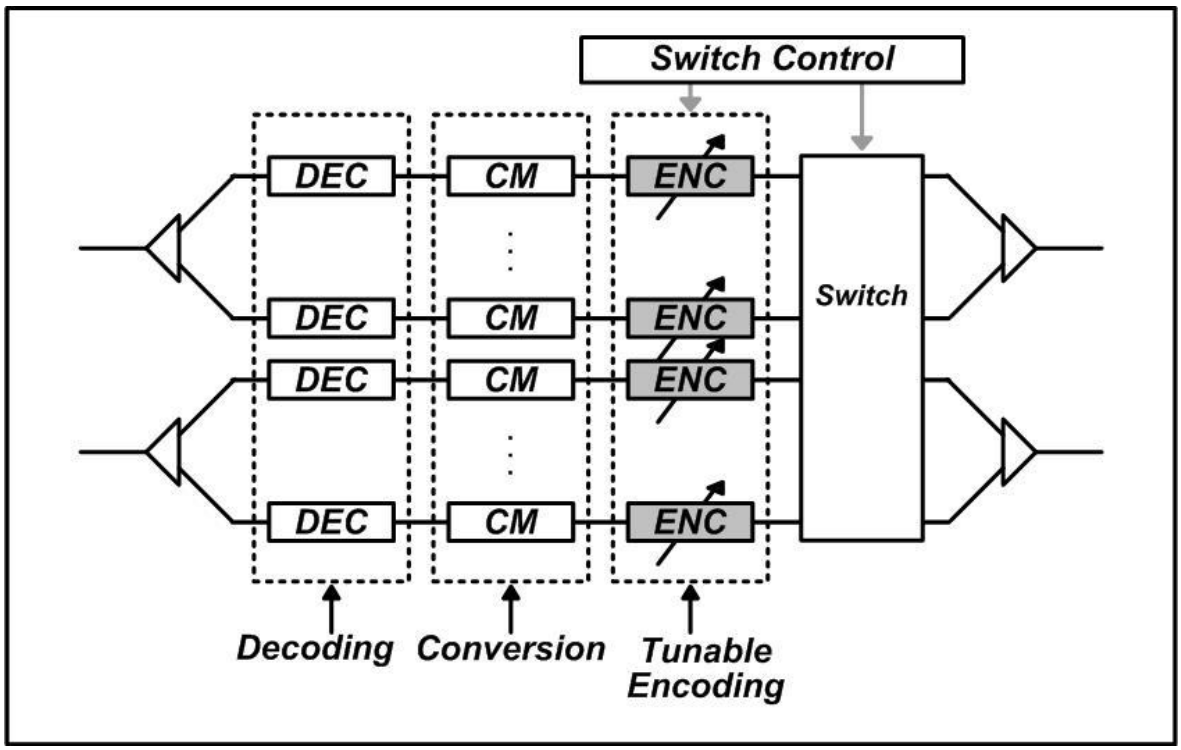

FIG. 2 (C) Alternative router node switching architecture

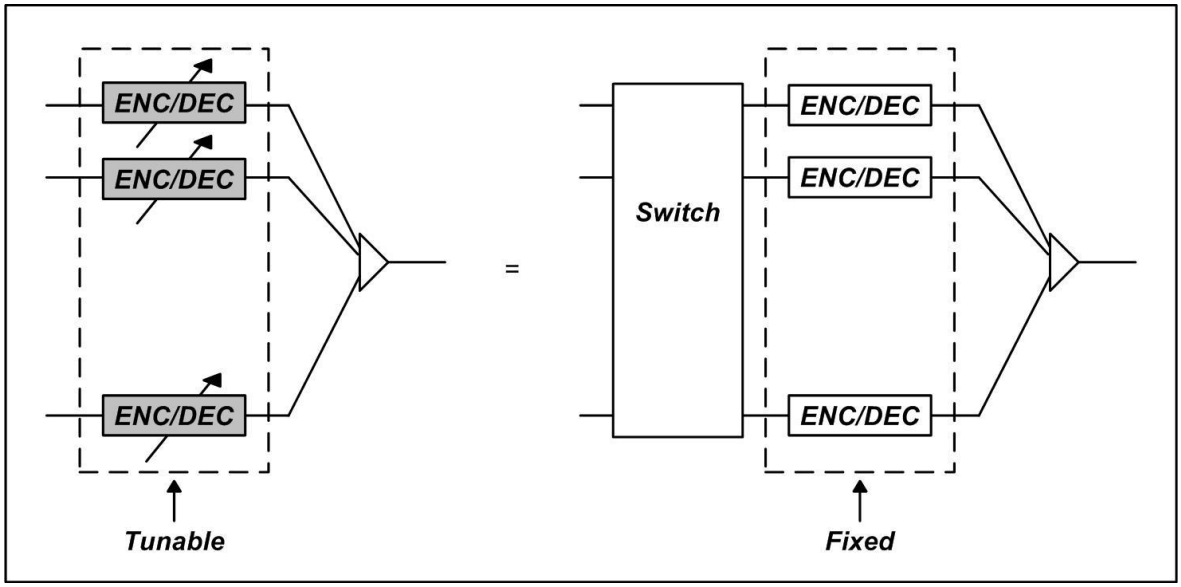

FIG. 3 The functional equivalence of encoder/decoder tunability and switching prior to the encoding/decoding stage

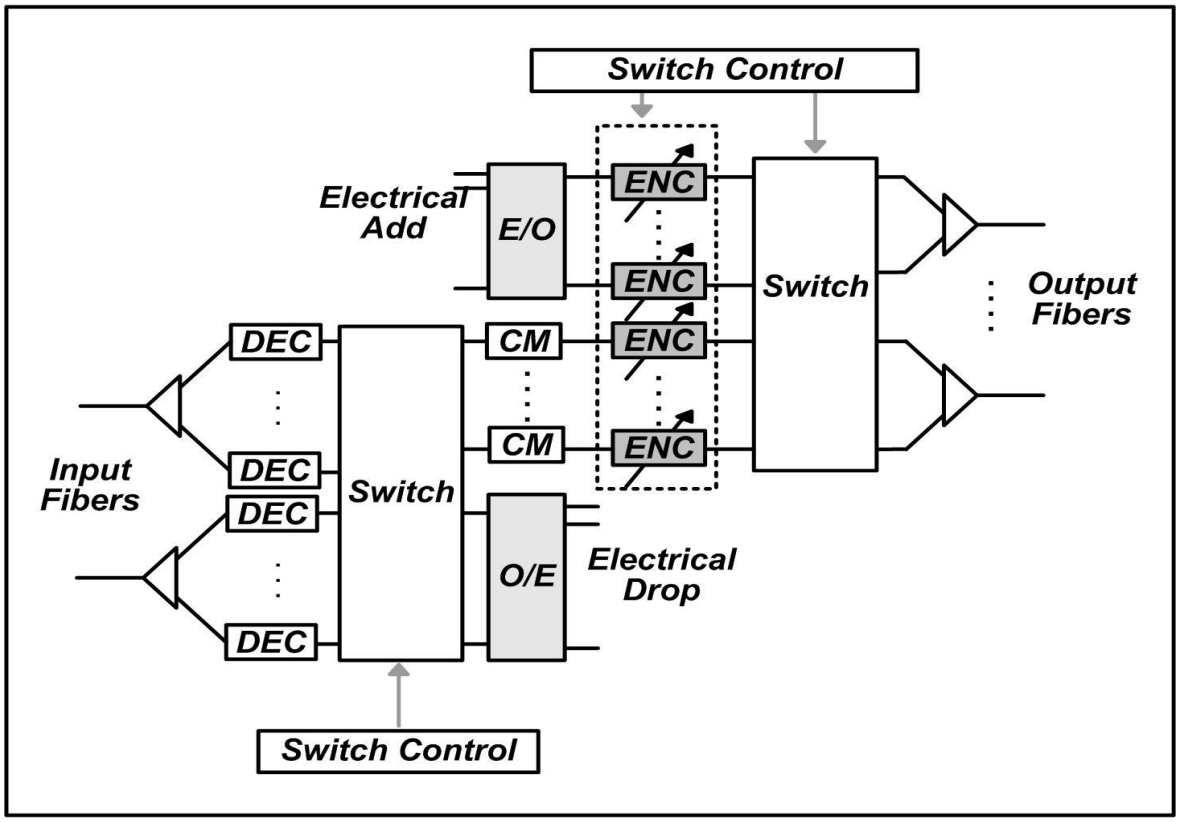

FIG. 4 (A) Edge node architecture

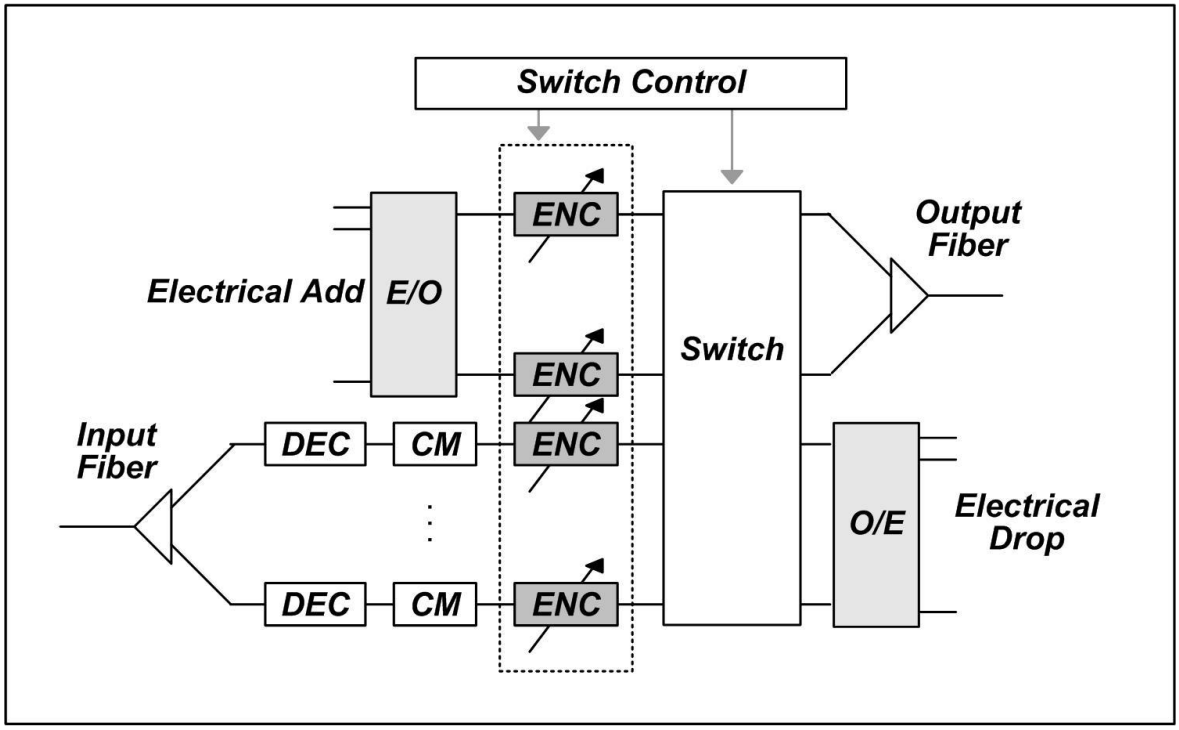

FIG. 4 (B) Alternative edge node architecture

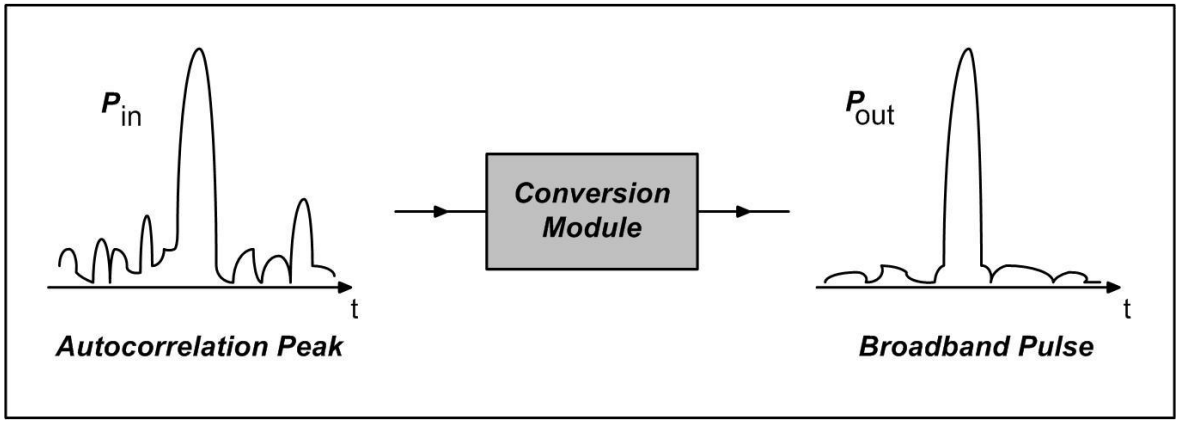

FIG. 5 (A) Conversion module (CM) block diagram

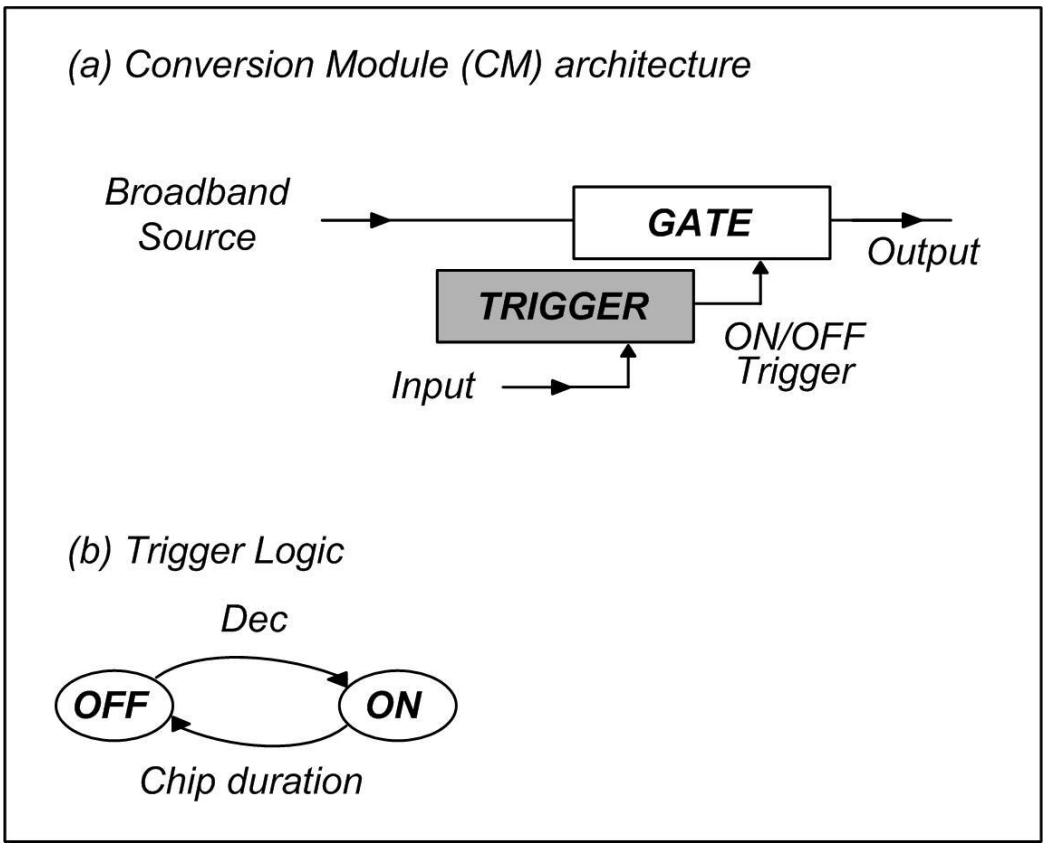

FIG. 5 (B) CM architecture

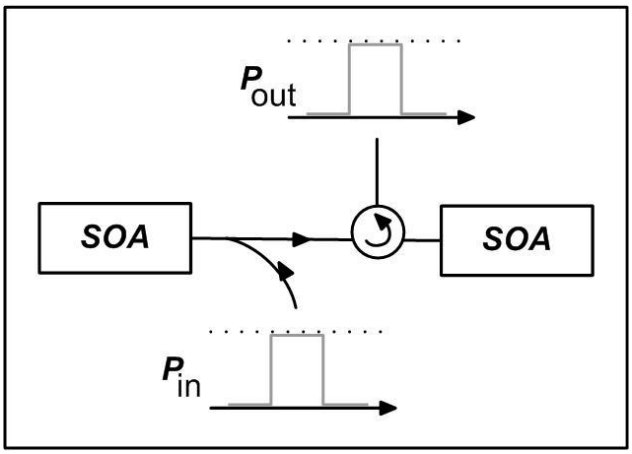

FIG. 5 (C) Possible CM implementation

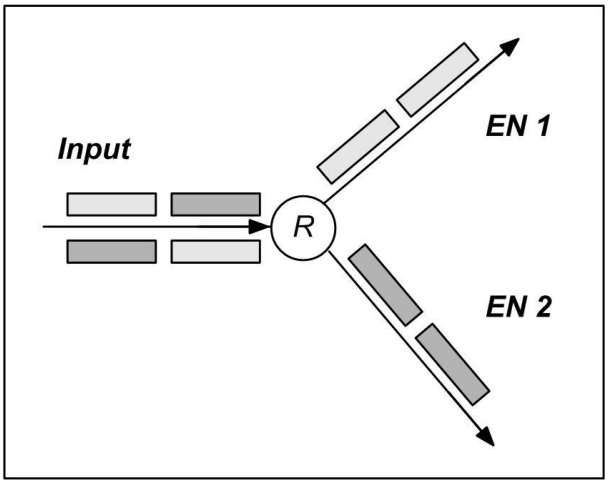

FIG. 6 (A) Packet Routing

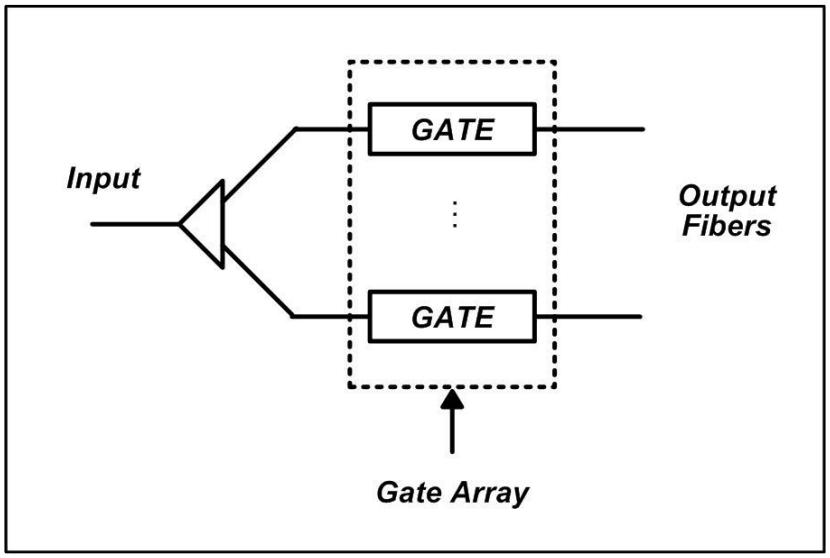

FIG. 6 (B) router with packet gate architecture

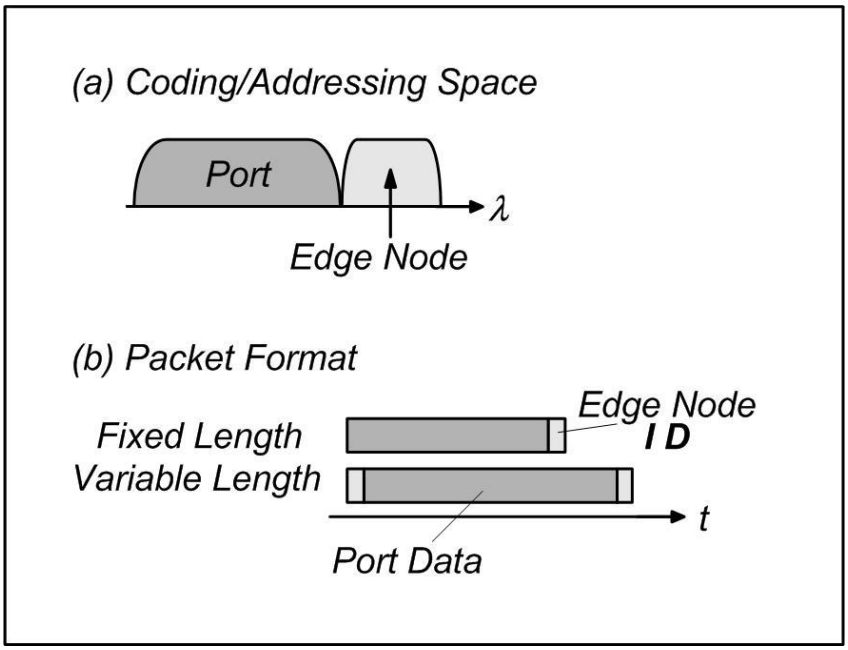

FIG. 7 (a) Addressing space and (b) Packet Format

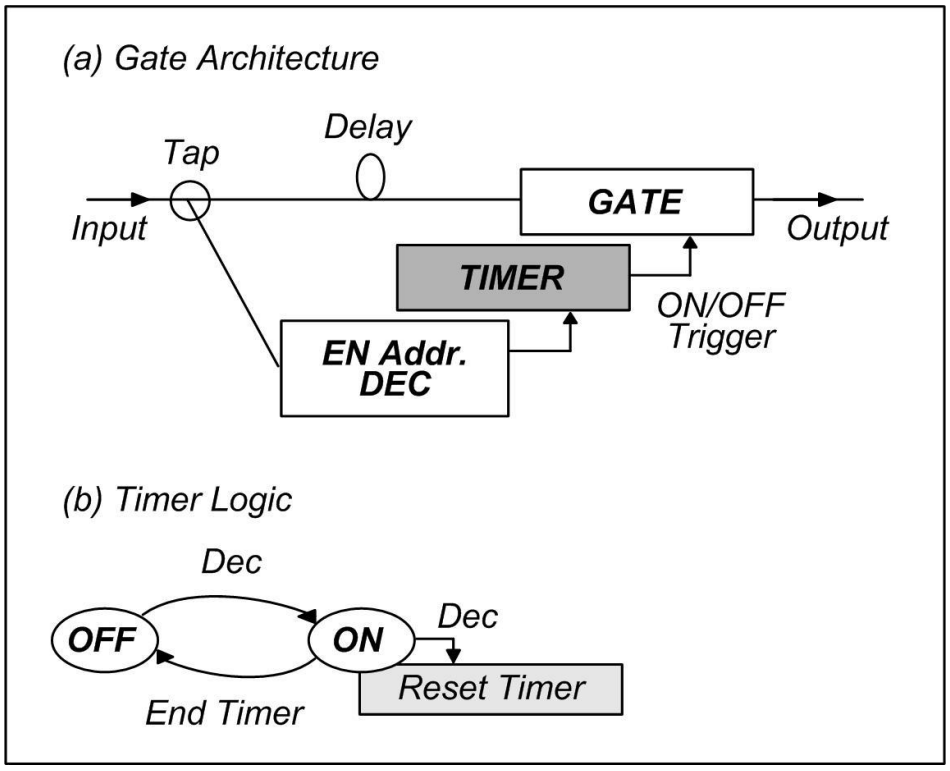

FIG. 8 Fixed-duration Packet Gate

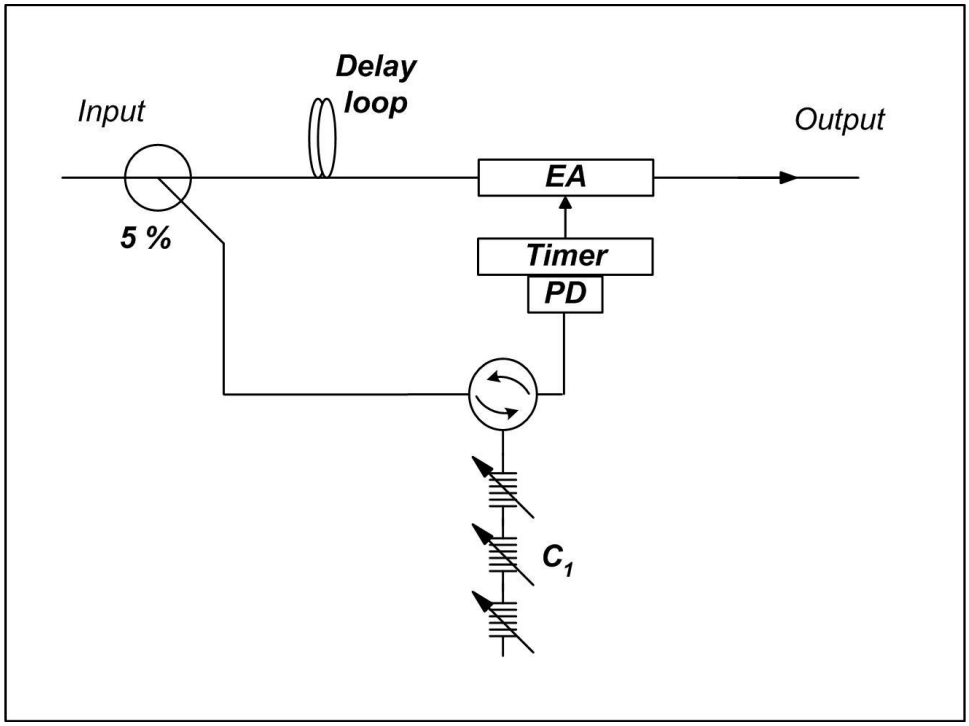

FIG. 9 Fixed-duration Packet Gate Implementation

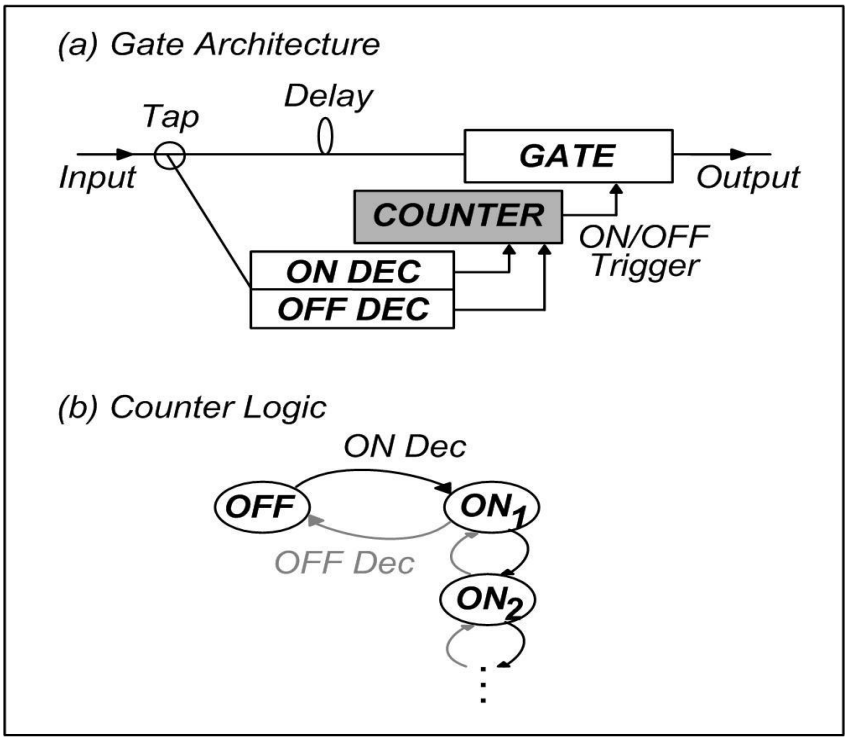

FIG. 10 Variable-duration Packet Gate

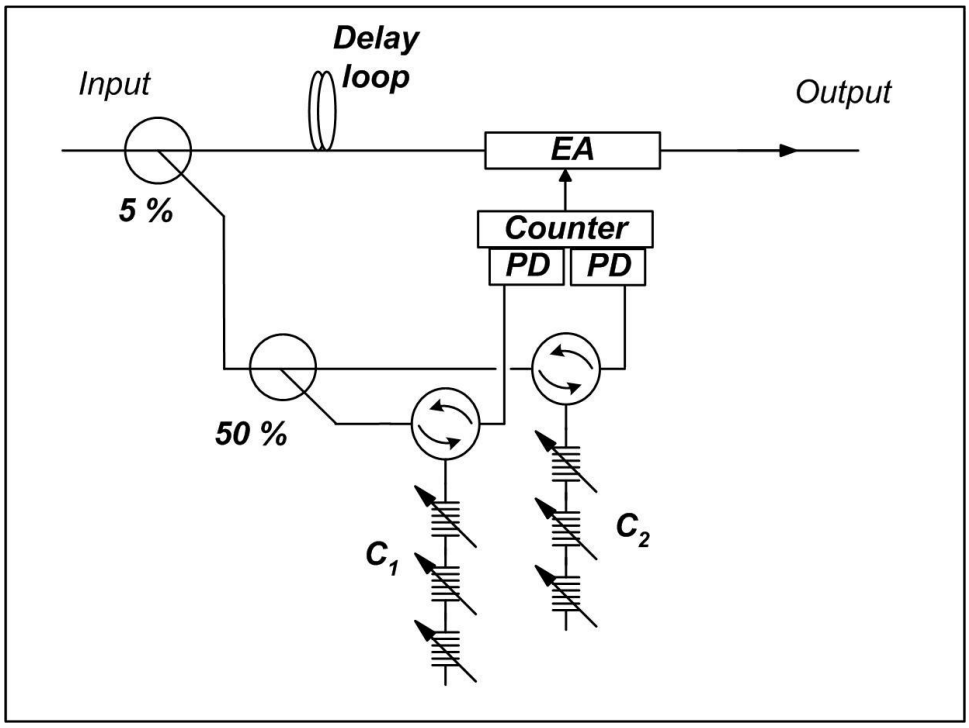

FIG. 11 Variable-duration Packet Gate Implementation

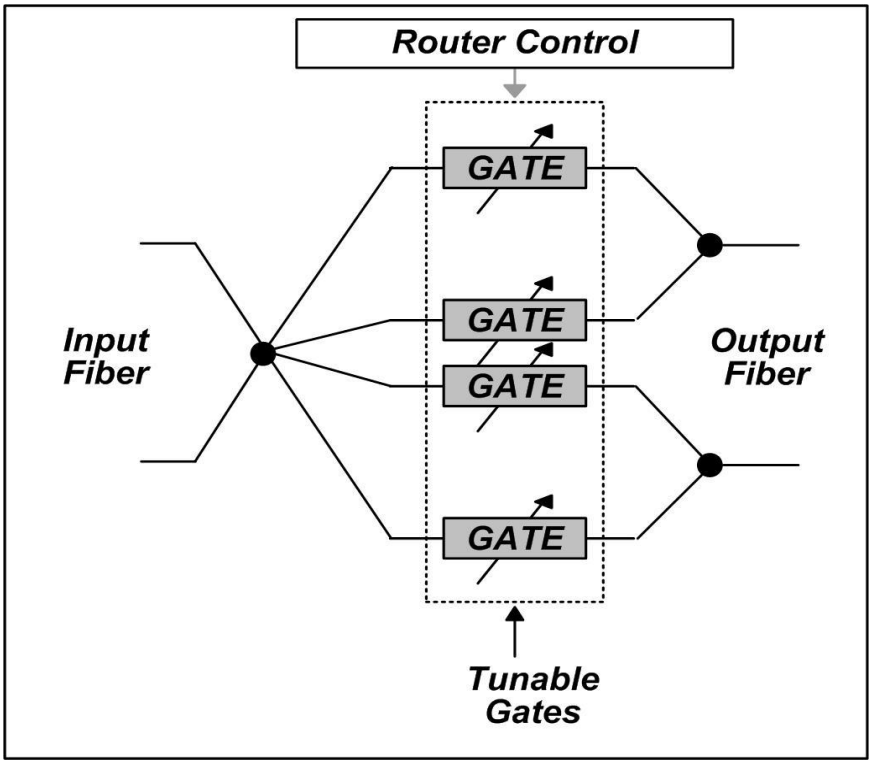

FIG. 12 All-optical Packet Router Based on Tunable Gate Arrays

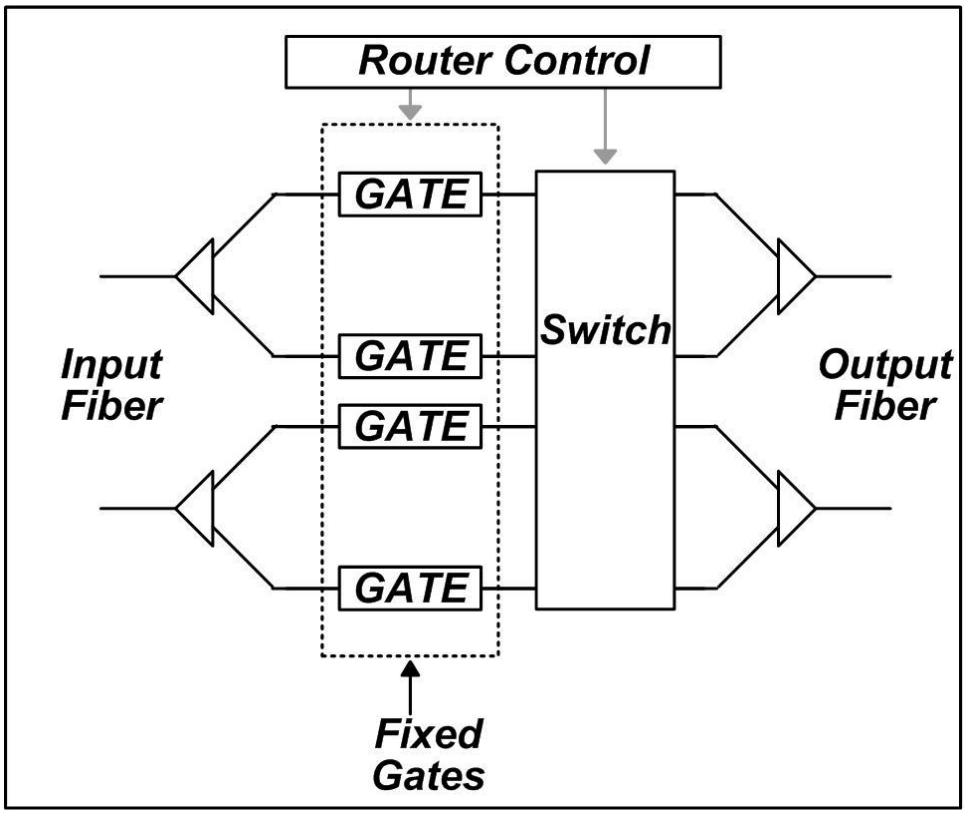

FIG. 13 All-optical Packet Router Based on Fixed Gate Arrays

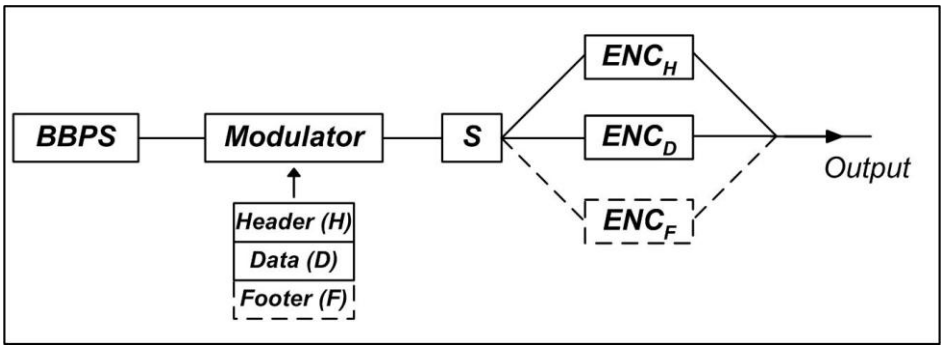

FIG. 14 Block Diagram for OCDM Packet Transmitter

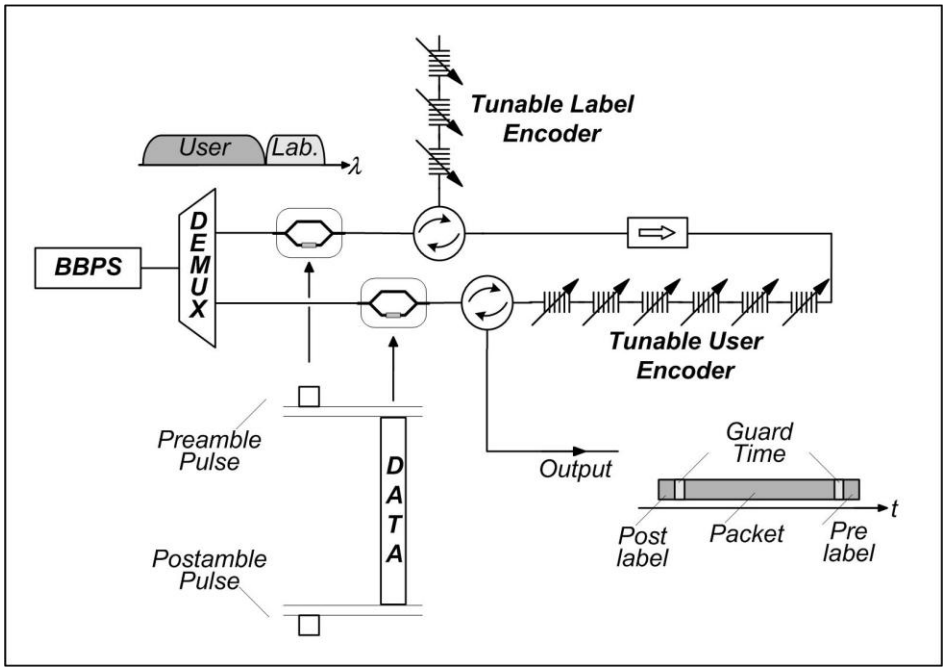

FIG. 15 Transmitter Configuration with Header/Footer Implementation

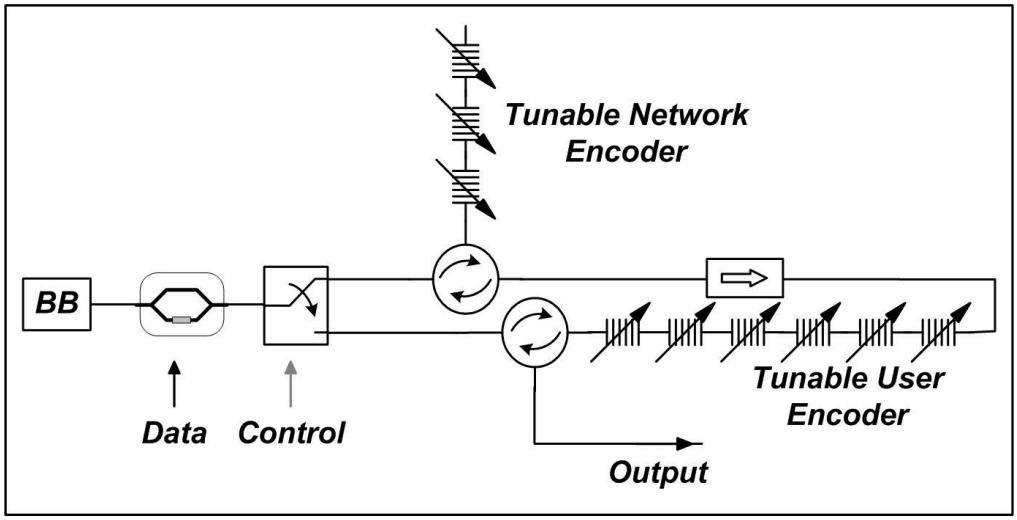

FIG. 16 Transmitter Configuration with Modulator/Switch

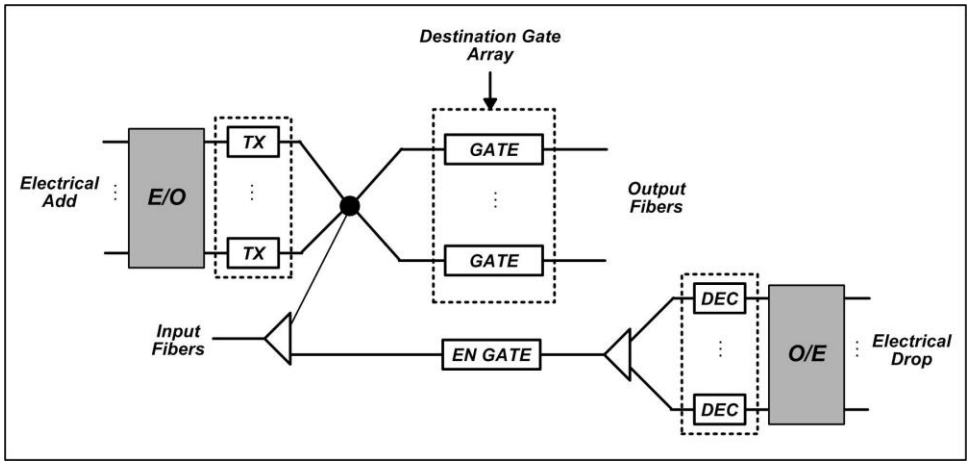

FIG. 17 Edge-Node for Packet-Switched Network

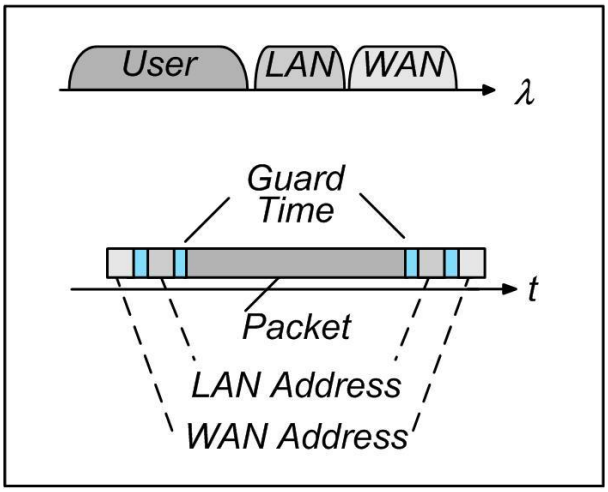

FIG. 18 3-Level Addressing Space and Packet Format

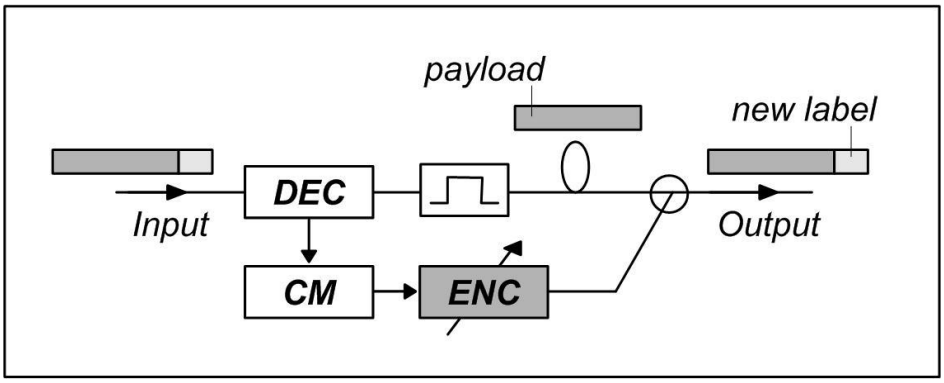

FIG. 19 Photonic Label Swapping (Fixed packet duration)

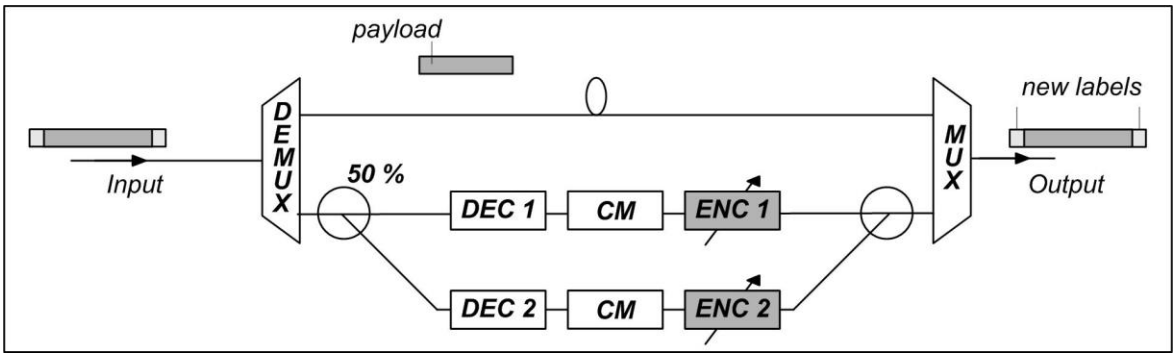

FIG. 20 Photonic Label Swapping (Variable packet duration).

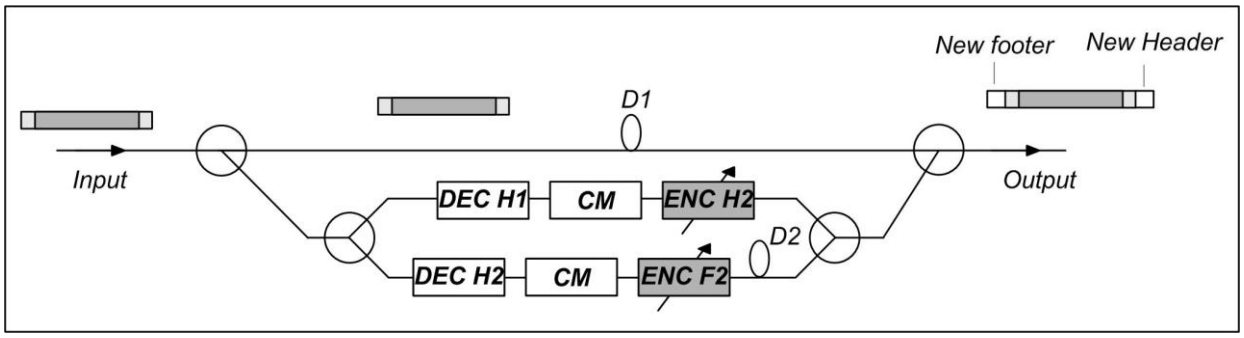

FIG. 21 All-optical CDM Packet Encapsulation