Embedded Data Flow Processing For Burst-Mode OLT/ONT PON System

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Abstract:

Burst mode data transfer in emerging wavelength division multiplexing (WDM) and code division multiplexing (CDM) PONs faces major challenges in electronics design. We develop an embedded software solution to enable optical line terminals (OLT) and Optical network terminals (ONT) to process Burst mode data flow smoothly. Our solution implements three important components on an FPGA platform. The first consists of a PCI interface that allows the OLT/ONT unit to communicate with a PC. The second is the PowerPC that manages and controls the data flow. Finally, a burst mode transceiver examines data transaction, synchronization and error correction.

Burst Mode Transciever (VHDL)

- Burst mode data transmission and reception
- Rocket IO interface
- Forward Error Correction (FEC)
- Packet formation, processing and buffering

PowerPC Control Firmware (C)

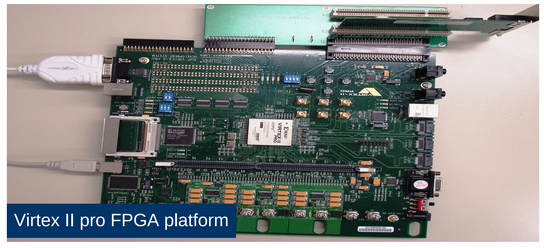
- Microcontroller program written in C
- Central control for the Prompt OLT/ONT
- Management of data flow between PCI interface and the burst mode transciever

Tools used for implementaion and testing

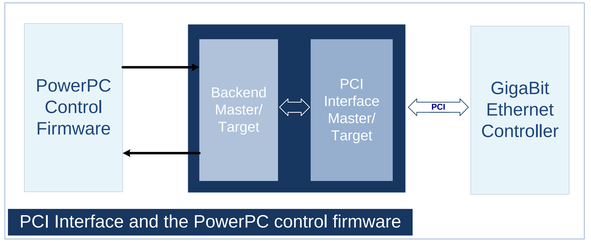
- Xilinx Virtex II pro (PowerPC)
- Xilinx ISE and XPS development environments
- Gigabit Ethernet controller

PCI Interface Core (VHDL)

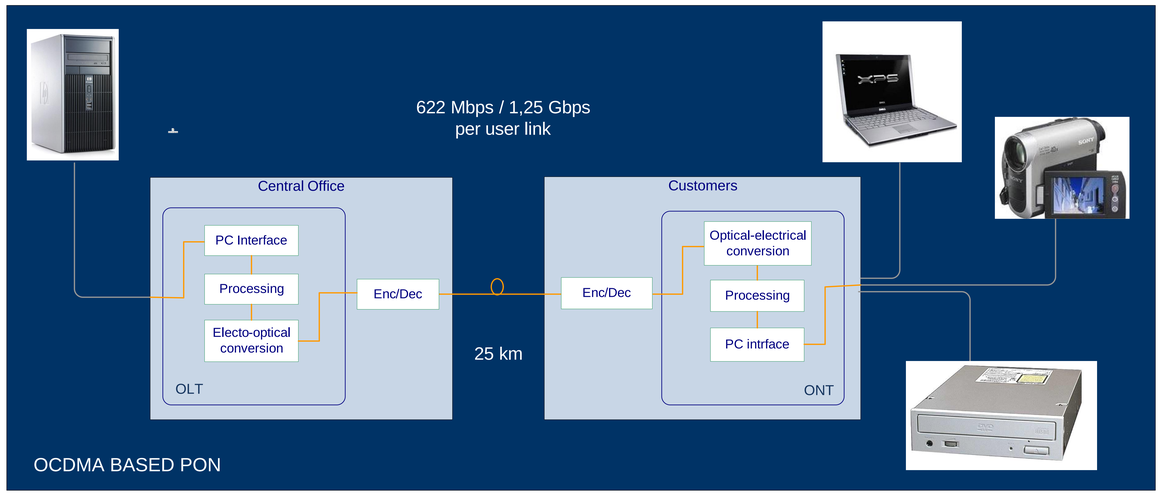
- PCI protocol implementation (PCI Interface)
- Backend interface
- Communication with PC using Gigabit Ethernet controller

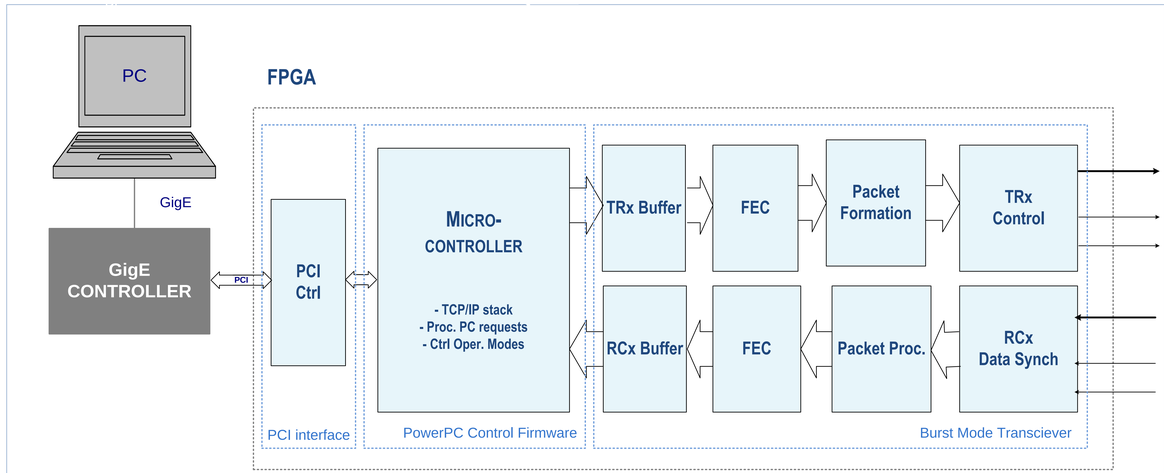


Virtex II pro FPGA platform



PCI Interface and the PowerPC control firmware





Transmitter/Receiver Block Diagram