**KING SAUD UNIVERSITY**

**COLLEGE OF COMPUTER AND INFORMATION SCIENCES**

Department name: Computer Engineering

Course Code & Title: CEN 215 LAB

Lab Instructor: Eng. Mohamed A. EZZAT.

Academic Year: 1438 / 1439h Semester: FIRST Semester

**SECTION I: LAB DEFINITION:**

**Lab Objectives:**

• To provide fundamental proficiency in logic design.

• Be able to simplify Boolean expressions using Boolean algebra and K-map.

• Be able to design small combinational and sequential circuits.

• Be able to build and test simple combinational and sequential circuits using IC chips.

**Subject Contents:**

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| --- | --- | --- |
| Points | Required Tasks | Working Week |
| 0 | Introduction. | 1 |
| 4 | Experiment 1: Introduction to Logic Gates. | 2 |
| 4 | Experiment 2: Combinational Logic Design with NAND & NOR Implementations. | 3 |
| 4 | Experiment 3: Combinational Logic Design with MSI Decoders. | 4 |
| 4 | Experiment 4: Combinational Logic Design with MSI Magnitude Comparator, Decoders and Multiplexers. | 5 |
| 20 | Mid-Term: Combinational Circuits. | 6 |
| 4 | Experiment 5: Sequential Circuits  Latches & Flip-Flops and Sequential Circuits Analysis. | 7 |
| 4 | Experiment 6: Sequential Circuits Design. | 8 |
| 4 | Experiment 7: Sequential Circuits Design. | 9 |
| 4 | Experiment 8: Advanced Sequential Circuits Design. | 10 |
| 8 | Experiment 9 & 10: project. | 11 |
| 40 | Final Exam: Sequential Circuits | 12 |

**Course Policies:**

1. Every week, the new experiment will be posted at the instructor page.

Complete the required task before coming to lab or you may be denied to perform the

experiment, you did not prepare, at the lab:

|  |
| --- |
| Required Tasks |
| The Truth Tables |
| K-Maps |
| Your design using Work Bench (Hard Copy) |
| Your design using Work Bench (Soft Copy) |

1. Each student is required to do his own work. Any academic irregularity (i.e. cheating) will not be tolerated and will result in a 0 on that lab experiment.
2. Your lab sessions are precisely 2 hours long. You will be given no extra time.
3. You must show up within the first 10 minutes of your lab starting time, **otherwise you will be considered ABSENT for that day**.
4. Lab experiments must be done at scheduled times.
5. Leave your working place in a good state, turn off equipment as appropriate, **otherwise you will get ZERO for that experiment.**
6. We will use e-mail for important announcements; **make sure you update your e-mail address in the group and check your e-mail on regular bases.**

**Grading policy:**

|  |  |
| --- | --- |
| Marks | |
| 32 marks (4 marks for each of 8 experiments)  ( 2 marks for experiment complete EWB designs +  2 marks for experiment successful board  implementation ) | Experiments |
| 20 marks | Mid-Term I |
| 8 marks | Project |
| 40 marks | Final Exam |

**SECTION II: Lab Introduction:**

**IMPORTANT INTRODUCTORY REMARKS:**

**Integrated Circuits**

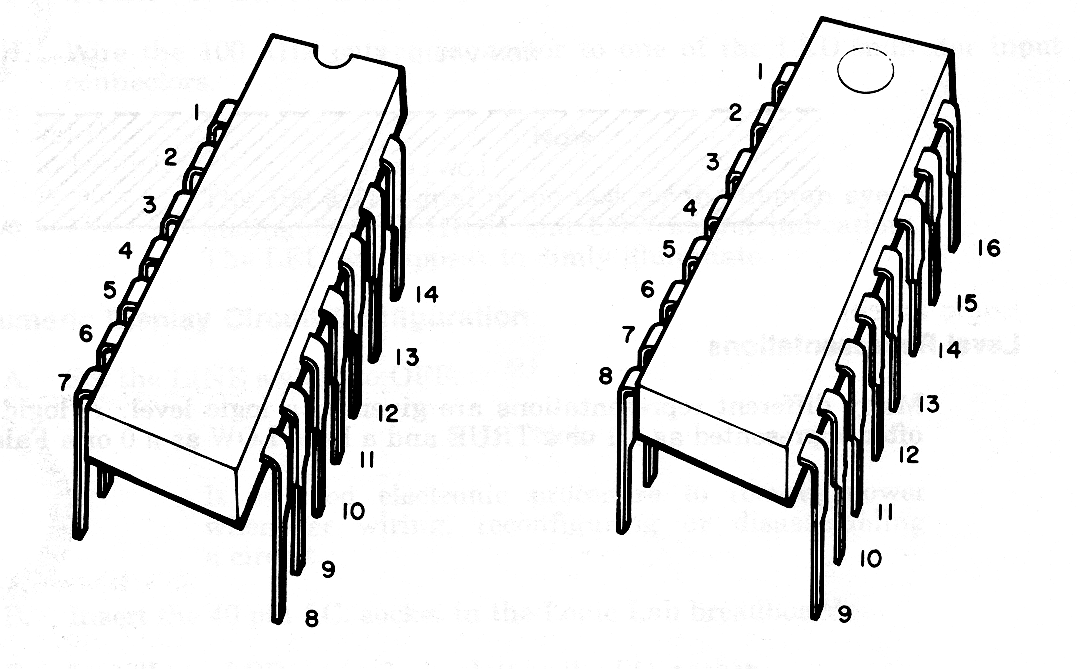
That course will be structured around the 74XX TTL (Transistor/Transistor Logic) series of integrated circuits, one of the most widely used general purpose logic families available today. These logic ele­ments have been incorporated into 14, 16 and in some cases larger packages depending on the logic functions) and the number of inputs provided. The abbreviation commonly used for the in-line style integrated circuit package is DIP for dual in-line package.

**Package Configuration**

The standard pin numbering of the 74XX series integrated circuit (I.C.)

Is determined as follows:

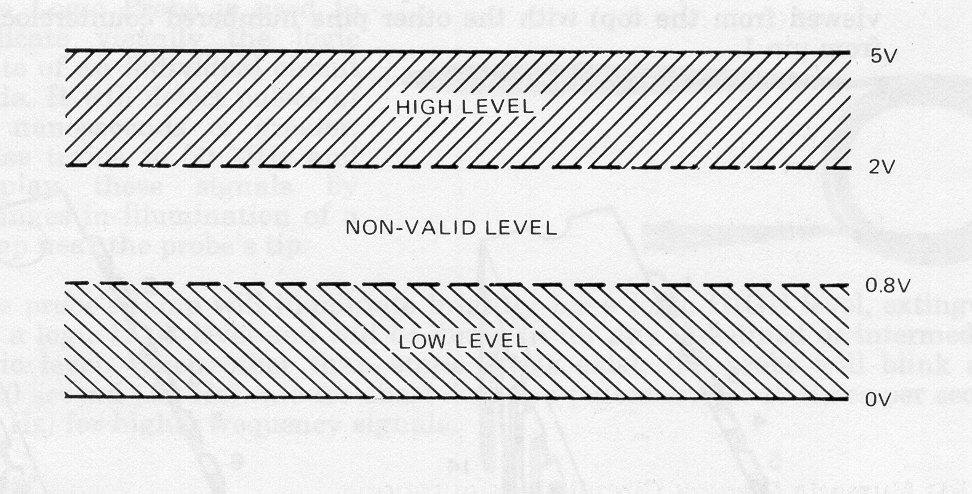
*Pin 1 is indicated by an indentation or other representative mark at the pin 1 end of the DIP. Pin 1 is the first pin counter clockwise from the mark (when viewed from the top) with the other pins numbered counter clockwise (CCW) from pin 1.*



Standard Package Configuration

**Logic Level Definition**

In most digital circuits only two logic levels are allowed to exist and within each logic family these levels are very rigidly defined. In the TTL family a logic HIGH is defined as any voltage level between 2~5V and a logic LOW as any voltage between 0-0.8V. The following illustration will give a pictorial representation of the TTL logic levels:



**Level Representations**

Many different representations are given to a logic level. A logic HIGH is often represented as a 1 or a TRUE and a logic LOW as a 0 or a False.

**Digital Troubleshooting Instrumentation**

***Logic Probe***

The Logic Probe is used to indicate visually the logic state of an individual circuit node. It will detect pulses of 30 nanoseconds, pulse trains to 17 M Hz. Three LED’s are used to indicate the logic level of the tested point:

* The Green LED is ON if the measured logic level is “LOW”.
* The Red LED is ON if the measured logic level is “HIGH”.
* The Yellow LED is ON if the measured logic level is “NON-VALID”.

Logic probe (type 1)

***Logic Clip***

The Logic Clip is a digital test instrument which may be clipped to any 14 or 16 pin integrated circuit (I.C.)to display the Logic levels of all pins simultaneously. A logic HIGH state is indicated by an illuminated LED and a logic LOW state by an extinguished LED. The clip requires no external power source because it is energized by the integrated circuit being tested.

