# **Experiment** **5**

**Sequential Circuits**

# **Latches & Flip-Flops and Sequential Circuits Analysis**

**A-Latches & Flip-Flops**

**Basic Concepts**

The storage elements are circuits that are capable of storing binary information. The binary information stored in these elements at any given time defines the *state* of the sequential circuit at that time. A storage element can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch its state. The most basic storage elements are *latches*, from which *flip-flops* are usually constructed.

**Latches**

The basic memory elements used in clocked sequential circuits are called latches. These circuits are binary cells capable of storing one bit of information. A latch circuit maybe constructed from two NOR gates as illustrated in Figure 1. It is called an SR (set-reset) latch. The circuit has two inputs S and R and two outputs Q and Q' (complement of Q).

|  |  |  |  |
| --- | --- | --- | --- |
| S | R | Q | Q’ |
| 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |

Figure 1: SR latch with NOR Gates

If S=1 and R=0 are, the Q output would be set to 1; if S=0 and R=1, the Q output would be reset to 0; if S and R at 0, the circuit output would be kept as been before; if S=1, R=1 the output of the latch goes to an unpredictable state. The truth table for the circuit can be checked for the given circuit design.

The operation of the basic NOR (and NAND) latches can be modified by providing an additional control input that determines when the state of the latch can be changed. By adding gates to the inputs of the basic circuit, the latch can be made to respond to input levels during the occurrence of the clock pulses. The clocked SR latch shown in figure 2. It consists of the basic NOR latch and two additional AND gates. The control input clock pulse (CP) acts as an enable signal for the other two inputs. The outputs of the two AND gates remain at 0 as long as the CP is 0, regardless of the S and R input values. When the clock pulse goes to 1, information from S and R inputs is allowed to reach the basic latch. The set state is reached with S=1, R=0 and CP=1. To change to the clear state inputs must be S=0, R=1 and CP=1.

|  |  |  |  |
| --- | --- | --- | --- |
| Q | S | R | Q(t+1) |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | Indeterminate |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | Indeterminate |

Figure 2: Clocked SR Latch

Note that the problem with the latch is that it is *transparent*: While the clock pulse is at logic 1, the state may keep changing and continue to change until the clock returns to 0. The final state depends on how long the clock pulse stays at the logic-1 level. This behavior is clearly unacceptable. The desired behavior is that the state changes only once per clock pulse. Therefore, the commonly-used solutions replace the clocked latches with *flip-flops.*

**Flip-Flops**

The key to the proper operation of flip-flops is to prevent them from being transparent. The flip-flops do not go through multiple changes of state per clock pulse. There are two ways to form flips-flops which are:

* Master-slave flip-flops.
* Edge-triggered flip-flops.

**Master-Slave Flip-Flops:**

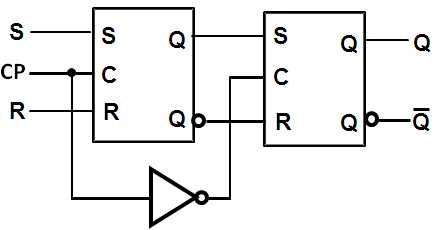
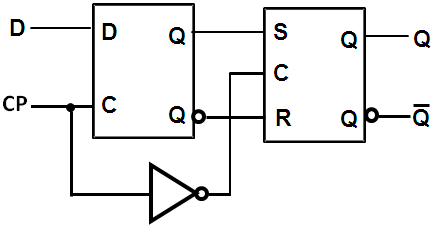
A master-slave flip-flop consists of two clocked SR latches in series  
with the clock on the second latch inverted as shown in Figure 3. The input is observed by the first latch with CP = 1 and the output is changed by the second latch with CP = 0.

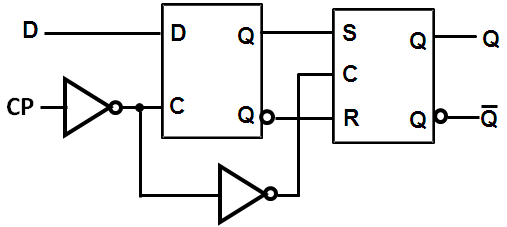
Figure 3: SR Master-Slave Flip-Flop

**Edge-Triggered Flip-Flops:**

An edge-triggered flip-flop ignores the pulse while it is at a constant level and triggers only during a transition of the clock pulse. Edge-triggered flip-flops can be built directly at the electronic circuit level, or a master-slave D flip-flop which also exhibits edge-triggered behavior can be used as shown in Figure 4.



(a) Negative-Edge-Triggered



(b) Positive-Edge-Triggered

Figure 4: Edge-Triggered D Flip-Flop

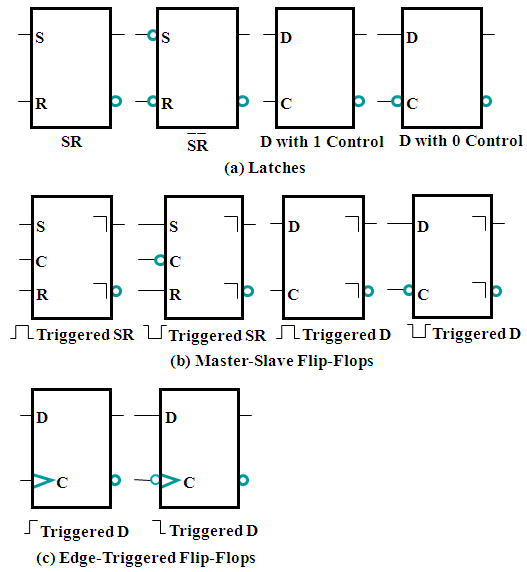
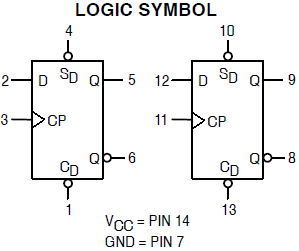
The standard graphic symbols for the different types of latches and flip-flops are shown in Figure 5.

Figure 5: Standard Graphic Symbols for Latches and Flip-Flops

**Dual D-Type Positive Edge-Triggered Flip-Flop:**

The 74LS74A offers dual edge-triggered flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and Q outputs. Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. The logic symbol and truth table of 74LS74A is shown in Figure 6.



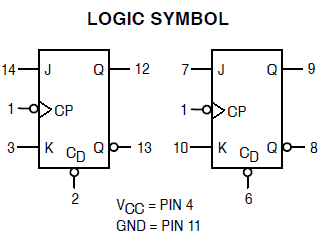
**TRUTH TABLE**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SD'** | **CD'** | **D** | **Q** | **Q'** | **Description** |
| **L** | **H** | **X** | **H** | **L** | **Asynchronously Set** |
| **H** | **L** | **X** | **L** | **H** | **Asynchronously Clear** |
| **L** | **L** | **X** | **H** | **H** | **Undetermined** |
| **H** | **H** | **H** | **H** | **L** | **Load 1 (Set)** |
| **H** | **H** | **L** | **L** | **H** | **Load 0 (Reset)** |

Figure 6: 74LS74A

**Dual JK Negative Edge-Triggered Flip-Flop:**

The 74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bi-stable electronic circuit will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse. The logic symbol and truth table of 74LS73A is shown in Figure 7.

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**TRUTH TABLE**

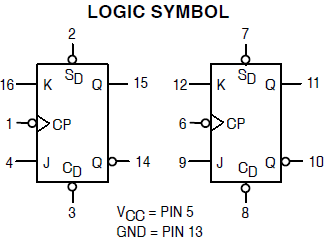
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **CD'** | **J** | **K** | **Q** | **Q'** | **Description** |
| **L** | **X** | **X** | **L** | **H** | **Asynchronously Clear** |
| **H** | **L** | **L** | **Q** | **Q'** | **No Change** |
| **H** | **L** | **H** | **L** | **H** | **Load 0 (Reset)** |
| **H** | **H** | **L** | **H** | **L** | **Load 1 (Set)** |
| **H** | **H** | **H** | **Q'** | **Q** | **Complement** |

Figure 7: 74LS73A

**Dual JK Flip-Flop With Set and Clear:**

The 74LS76A offers individual J, K, Clock Pulse, Direct Set and Direct Clear inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The Logic Level of the J and K inputs will perform according to the Truth Table as long as minimum set-up times are observed. Input data is transferred to the outputs on the HIGH-to-LOW clock transitions, negative edge. The logic symbol and truth table of 74LS76A is shown in Figure 8.

**TRUTH TABLE**

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **SD'** | **CD'** | **J** | **K** | **Q** | **Q'** | **Description** |
| **L** | **H** | **X** | **X** | **H** | **L** | **Asynchronously Set** |
| **H** | **L** | **X** | **X** | **L** | **H** | **Asynchronously Clear** |
| **L** | **L** | **X** | **X** | **H** | **H** | **Undetermined** |
| **H** | **H** | **L** | **L** | **Q** | **Q'** | **No Change** |
| **H** | **H** | **L** | **H** | **L** | **H** | **Load 0 (Reset)** |
| **H** | **H** | **H** | **L** | **H** | **L** | **Load 1 (Set)** |
| **H** | **H** | **H** | **H** | **Q'** | **Q** | **Complement** |

Figure 8: 74LS76A

**Procedure**

**Part 1:**

Using Workbench, connect the circuit of figure 1 and verify the characteristic of an SR latch.

**Part 2:**

Using Workbench, connect the circuit of figure 2 and verify the characteristic of a clocked SR latch.

**Part 3:**

Using Workbench, use 74LS74A and verify the characteristic table of D-type positive edge-triggered flip-flop

**Part 4:**

Using Workbench, use 74LS76A and verify the characteristic table of JK negative edge-triggered flip-flop

**Part 5 (Workbench and Implementation):**

A set-dominant master-slave flip-flop has set and reset inputs. It differs from a conventional master-slave *SR* flip-flop in that, when both *SD* and *RD* are equal to 1, the flip-flop is set.

1. Design theset-dominant positive edge-triggered flip-flop by EWB & using IC 74LS74A.

|  |  |  |  |
| --- | --- | --- | --- |
| **SD** | **RD** | **Q(t)** | **Q(t+1)** |
| **0** | **0** | **0** |  |
| **0** | **0** | **1** |  |
| **0** | **1** | **0** |  |
| **0** | **1** | **1** |  |
| **1** | **0** | **0** |  |
| **1** | **0** | **1** |  |
| **1** | **1** | **0** |  |
| **1** | **1** | **1** |  |

D =

Clock

SD

RD

?

?

1. Design theset-dominant positive edge-triggered flip-flop by using EWB & IC 74LS76A.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SD** | **RD** | **Q(t)** | **Q(t+1)** | **J** | **K** |
| **0** | **0** | **0** |  |  |  |
| **0** | **0** | **1** |  |  |  |
| **0** | **1** | **0** |  |  |  |
| **0** | **1** | **1** |  |  |  |
| **1** | **0** | **0** |  |  |  |
| **1** | **0** | **1** |  |  |  |
| **1** | **1** | **0** |  |  |  |
| **1** | **1** | **1** |  |  |  |

J =

K =

Clock

SD

RD

?

?

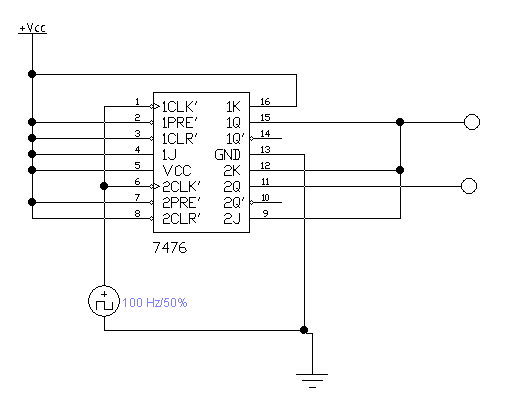
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* **Choose one of part A or B designs and implement it on your board.**

**B- Sequential Circuits Analysis:**

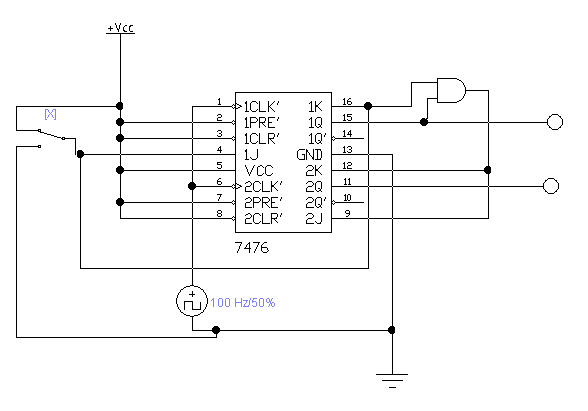
**Procedure I:**

Find the **state table** for the following circuit then, summarize the main function of the design:



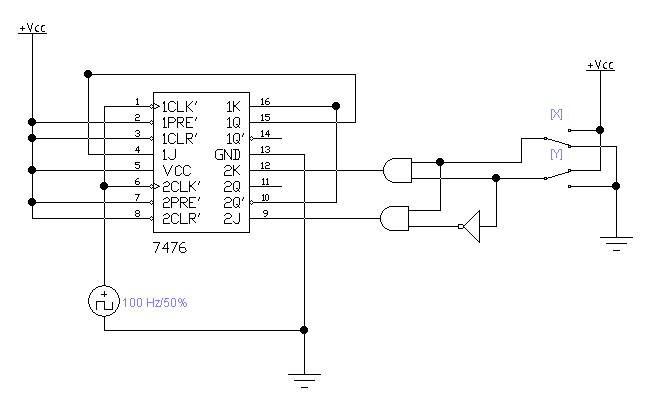
**Procedure II:**

Find the **state table** for the following circuit then, summarize the main function of the design:



**Procedure III:**

Find the **state table** for the following circuit then, summarize the main function of the design:

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**Procedure IV:**

Choose one of the above three designs and simulate it on board and show the decimal equivalent of Q1Q2 for every clock pulse on one of your board’s seven segment displays.