# **Experiment 6**

# **Sequential Circuits Design**

**Objective:**

* To understand the design principles of sequential circuits.
* Design simple counters and sequential circuits.

**Basic Concepts:**

As you have seen in the previous lab, design of a sequential circuit starts from a set of specifications and results in a list of Boolean functions from which the logic diagram can be obtained. Sequential circuits require a state table or state diagram for its specification. Such circuits require a set of flip flops and a combinational logic to fulfill the specifications. The minimum number of flip-flops required for a synchronous sequential circuit is determined by the number of states in the circuit. N flip-flops can represent up to 2n binary states. The combinational logic is derived from the state table by evaluating the flip-flop input equations and output equations.

The design procedure consists of:

1. Specification.
2. Formulation of state table from problem statement.
3. Or: from the state diagram, derive the state table.
4. Flip-flop input equation determination from the present state entry, and excitation table in the state table.
5. Output equation determination from the output entries in the state table.
6. Optimize the flip-flop input and output equations.
7. Draw the logic diagram using flip-flops and logic gates.
8. Verify the correctness of the design, using EWB.

**Procedure I:**

1. Suppose we have a sequential lock circuit that have two inputs *x* and *y*, and a single output *z*. The output should be 1 if the *x y* input sequence 01, 11, 10 has been received and 0 otherwise.

Give a complete design procedure for the above lock using D F.F’s

and simulate it using EWB.

1. Give a complete design procedure for a 4-bit down counter using D flip-flops and then simulate it using EWB.
2. Give a complete design procedure for a BCD counter using JK flip-flops and simulate it using EWB.
3. Given a ring counter that goes through the following sequence:

0000 1000 110 0 1110 1111 0111 0011 0001 then repeats.

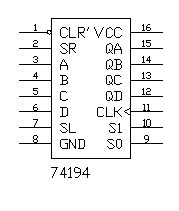
Give a complete design procedure using JK flip-flops and simulate it

using EWB.

1. Implement one of the above four designs on your board, according to lab instructor directions.

**Procedure II:**

Give a complete design procedure for the ring counter in procedure 1-4 using Shift Register (74194 IC) and then:



* Simulate it using EWB.
* **Implement design on your board.**
* Compare design in procedure I-4 to design in procedure II

in your report.

Function table for IC 74194: MBNMBJGHGG

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Mode | |  | Serial | | Paralle  M M l | | | | Outputs | | | |
| Clear | S1 | S0 | CLK | Left | Right | A | B | C | D | QA | QB | QC | QD |
| 0 | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 |
| 1 | X | X | 0 | X | X | X | X | X | X | QA | QB | QC | QD |
| 1 | 1 | 1 | Pos | X | X | a | b | c | d | a | b | C | D |
|  | 0 | 1 | Pos | X | 1 | X | X | X | X | 1 | QA | QB | QC |
| 1 | 0 | 1 | Pos | X | 0 | X | X | X | X | 0 | QA | QB | QC |
| 1 | 1 | 0 | Pos | 1 | X | X | X | X | X | QB | QC | QD | 1 |
| 1 | 1 | 0 | Pos | 0 | X | X | X | X | X | QB | QC | QD | 0 |
| 1 | 0 | 0 | X | X | X | X | X | X | X | QA | QB | QC | QD |

- POS = transition from low to high