**King Saud University**

**College of Computer and Information Sciences**

**Department of Computer Engineering**

**CEN 313 – LOGIC DESIGN AND HARDWARE DESCRIPTION LANGUAGES (3-0-1)**

**Semester II, Academic Year 2016-2017**

**Required Course: Time (1, 3, 5. 11:00-Noon)**

**Course Description (catalog):**

Programmable Logic Devices (PLDs): architecture, features, timing parameters, configuration. Hardware Description Languages (HDLs): History, purpose, categories, vendors and associated CAD tools. Verilog: constructs, modeling for simulation, synthesis and verification, coding styles, effect of style on synthesis, synthesis of combinational and sequential logic, capabilities to deal with hierarchy, subprograms, test benches.

**Prerequisites: - Courses** CEN214

* Topics
* Design and analysis of combinational logic circuits
* Design and analysis of sequential logic circuits

**Textbook(s) and/or Other Required Materials:**

**Primary:** Samir Palnitkar, *Verilog HDL* 2nd Ed. 2003, Prentice Hall.

**Supplementary:**

 Blaine Readler, *Verilog by Example: A Concise Introduction for FPGA Design*, 2011, Full Arc Press.

**Course Learning Outcomes:** This course requires the student to demonstrate the following:

1. Identify key features and uses of different HDLs and PLDs.
2. Apply high-level design languages and knowledge of Boolean algebra to define and develop digital modules.
3. Define and use the behavioral, dataflow and structural styles of writing HDL codes.
4. Discover practical issues in the design of complex digital systems using HDL.
5. Write functionally correct and well-documented HDL code intended for simulation and synthesis.

**Major Topics covered and schedule in weeks:**

|  |  |
| --- | --- |
| PLDs and CPLDs: comparing, contrasting and latest advances | 2 |
| Hardware description Languages: traditional and advanced | 1 |
| Introductory concepts in Verilog | 2 |
| Simulation cycle and related issues | 1 |
| Modeling and synthesis of Combinational and Sequential logic in Verilog | 3 |
| Hierarchy in large designs and resource utilization | 2 |
| Subprograms and test benches in Verilog | 2 |
| Review and evaluation | 2 |

**Assessment Plan for the Course**

Students’ performance in homework, quizzes, exams and class projects.

**Contribution of Course to Meeting Curriculum Disciplines:**

|  |  |
| --- | --- |
| **Curriculum Discipline** | **Percentage** |
| Mathematics and Basic Science |  |
| Engineering Science |  |
| Engineering Design | **100** |
| General Education |  |

**Relationship of Course to Student Outcomes**

|  |  |  |
| --- | --- | --- |
| **Outcome** | **Student Outcome Description** | **Contribution** |
| (a) | an ability to apply knowledge of mathematics, science, and engineering | ✓ |
| (b) | an ability to design and conduct experiments, as well as to analyze and interpret data |  |
| (c) | an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability | ✓ |
| (d) | an ability to function on multidisciplinary teams |  |
| (e) | an ability to identify, formulate, and solve engineering problems | ✓ |
| (f) | an understanding of professional and ethical responsibility |  |
| (g) | an ability to communicate effectively |  |
| (h) | the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context |  |
| (i) | a recognition of the need for, and an ability to engage in life-long learning |  |
| (j) | a knowledge of contemporary issues |  |
| (k) | an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice. | ✓ |

**Course Instructor, Department, Office Hours, Contact Information, and Course Offering Schedule:**

* Instructor: Dr. Mujahed Mekhallalati
* Lectures: 11:00am-11:50am (Sun, Tue, and Thus)
* Department: Computer Engineering
* Office: Room 2226, Building 31
* Office Hours: as displayed on office door
* E-mail: [mujahedm@ksu.edu.sa](mailto:mujahedm@ksu.edu.sa)

**Assessments weights and dates:**

Midterms (2) = 40%. 1st midterm 9th April 2017, 2nd midterm 30th April 2017.

Homeworks= 8%.

Pop Quizes =12% (best 4 results). Short tests given to students without any prior warning.

Final exam = 40% (Comprehensive exam)

**Additional Course Policies:**

Homework assignments are due one week from their assigned date. They will be collected at the beginning of the class period. NO late submissions will be accepted whatsoever. Further, students are expected to demonstrate classroom etiquette by observing the following principles:

1. Attending every lecture throughout the semester.
2. Arriving for every class on time so that the instructor may start and end class according to schedule.
3. Arriving for exams on time so that students can use all the allotted time.
4. During the class periods:

* Students should refrain from disruptive behavior such as holding side conversations and using smart phones, tablets, or laptops to surf the web or check e-mail.
* Students may use their laptops or tablets for note-taking ONLY during lectures.

1. Use of mobile phones, iPods, and tablets for communication purposes is not permitted during lecture. Students seen using any of these devices may be asked to leave the room for the balance of the lecture.

Prepared by Dr. Mujahed Mekhallalati