كلية الهندسة
جامعة الملك سعود
King Saud University
College Of Engineering

EE 312

Fundamentals of Electronics LAB

LAB Manual

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Version

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Course Policy

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Objective: To introduce the students to the basic electronic devices and their applications as well as building their circuit construction skills.

Grading Policy:

Participation and lab skills assessment	10%
Lab Work	20%
Homework+ two Comprehensive Reports / Presentation	20%
Midterm	20%
Final	30%

Lab Manual: http://faculty.ksu.edu.sa/almadhi/courses/Documents/ee312/EE312_Man.pdf

Course Schedule

Week No.	Activity	notes
	Lab 1	
	Lab 2	
	Lab 3	
	Lab 4	
	Lab 5	*Go to AC 123*
	Revision	Report 1
	Midterm Exam	
	Lab 6	
	Lab 7	
	Lab 8	
	Lab 9	
	Lab 10	
	Revision	Report 2
	Final Exam	

LAB 1

An Introduction to Semiconductor Diodes

1.1 Objective

- To identify the common types of semiconductor diodes.
- To learn the method of their testing.
- To explore their basic principle of operation.

1.2 Introduction

A p-n junction diode is a two-terminal electronic device which has important applications that we shall explore in this lab. The p-side of the junction is called the ***anode*** while the n-side is called the ***cathode*** (see Fig. 1a). The diode is characterized by a low resistance to current flow in the forward direction (into the anode and out of the cathode), and very high resistance in the reverse direction.

In dc circuits, a forward-biased diode can be approximately modeled by a constant voltage that depends on its type and characteristics. On the other hand, a reverse-biased diode can be modeled by an open circuit.

The *cathode* of a diode is usually marked by a band or a dot. It also can be identified based on a simple test using a digital multimeter (DMM). In that test, the diode is connected between the V Ω (red) and the COM (black) jacks of the DMM. With no device connected between its terminals, a DMM displays "**OL**" which is an indication of an open circuit.

If the DMM "OL" (open circuit) reading does not change upon connecting the diode ⇒ the diode is reverse-biased and acting as an open circuit; its *cathode* in this case is the lead connected to the V Ω (*red*) jack of the DMM.

If, however, the DMM displays a voltage drop upon testing the diode ⇒ the diode is forward-biased and its *cathode* is connected to the COM (*black*) jack (see Fig. 1b).

If the DMM displays "OL" or some low voltage drop in ***both*** directions ⇒ the diode is defective.

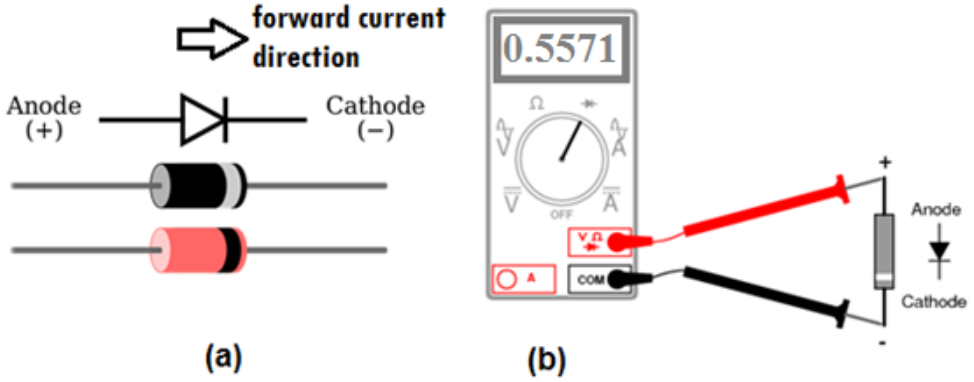


Figure 1 **(a)** Diode shape and symbol. **(b)** Testing a diode using a DMM.

1.3.1 Procedure A: How to Test a Diode

1. Set your DMM to diode-test mode.
2. Observe and record the open-circuit reading of the DMM in Table 1.
3. Connect any type of diode between the V (red) input jack and the COM (black) input jack of the DMM (Fig. 1b). Observe the DMM reading. Determine the cathode of each diode based on the approximate expected values given in Table 1. Record your measurements.

1.3.2 Procedure B: Diodes in Action

Make sure that your DMM is set to measure dc voltage.

1. Connect the circuit shown in Fig. 2.
2. Set V_{DD} to 4 V. Measure V_{AB} and $V_{1\text{-}k\Omega}$; record their values in Table 1.
3. Reverse the diode connection and repeat step 2.

Note: The voltage across the 1-k Ω resistor will give you an indication whether a current is actually flowing in the circuit or not. A higher voltage indicates a higher current (Ohm's law).

4. Repeat the previous steps for an LED.
5. Measure V_{AB} and $V_{1\text{-}k\Omega}$ after you connect two forward-biased silicon diodes between A and B in series.
6. Measure V_{AB} and $V_{1\text{-}k\Omega}$ after you connect two silicon diodes between A and B in series with their anodes connected together (back-back connection).
7. Measure V_{AB} and $V_{1\text{-}k\Omega}$ for a forward-biased silicon diode connected in parallel with a forward-biased LED between A and B. *Why doesn't the LED glow brightly?*

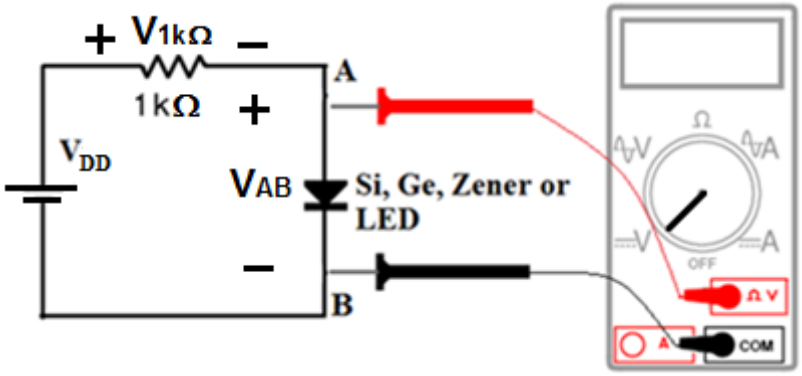


Figure 2 Exploring the behavior of semiconductor diodes.

1.4 Results

Table 1			
DMM reading in case of open circuit or reverse-biased diode:	Type of diode	DMM reading if the diode is forward-biased	
		expected	measured
	Si	0.55 ~ 0.75 V	
	Ge	0.2 ~ 0.4 V	
	Zener	0.55 ~ 0.75V	
	LED	1.5 ~ 3.5 V	

Table 2					
Step	Diode Type	Connection	V_{AB} (V)	$V_{1\text{-}k\Omega}$ (V)	Is there a current? (Yes/No)
1	silicon	forward			
2	silicon	Reverse			
3	LED	forward			
4	LED	Reverse			
5	2 silicon diodes in series	forward			
6	2 silicon diodes in series	back to back			
7	a silicon diode parallel with an LED	forward			

1.5 Homework

Write down a conclusion for this experiment. Your conclusion should cover the following:

- The general idea of procedure A as well as procedure B.
- The most important things you have learned from these two procedures.
- Any comments you would like to add.
- Suggest any steps of procedure you would like to add to this lab session and try to predict the outcome.

LAB 2

Diode Characteristics

2.1 Objective

- To experimentally obtain the i-v characteristic curves for two common diodes.
- To be able to extract a piecewise-linear model from a given i-v characteristic.
- To be able to estimate some physical constants from the obtained measurements.

2.2 Background

The relationship between a diode's current and its voltage takes the following form:

$$i = I_S(e^{\frac{v}{nV_T}} - 1) \qquad (1)$$

$$i_D \approx I_S e^{\frac{v_D}{nV_T}} \qquad (\text{for } v_D > 4V_T \approx 0.1\ V)$$

For a forward-biased diode, in order to change the current from I_{D1} to I_{D2}, we need to change its voltage by ΔV_D which can be calculated by:

$$\Delta V_D = V_{D2} - V_{D1} = nV_T \ln(\frac{I_{D2}}{I_{D1}}) = 2.3nV_T \log(\frac{I_{D2}}{I_{D1}}) \qquad (2)$$

from which one can deduce that in the forward bias region of operation, the voltage drop across a diode does not change that much even if the current passing through it changes significantly (why?).

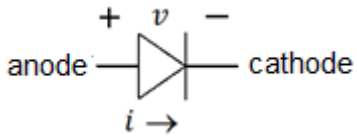


Figure 1 Reference current direction and voltage polarity.

2.3 Procedure

1. Measure and record the actual value of R. $R =$ kΩ

2. Connect the circuit shown in Fig. 2a. Set the dc supply voltage V_{DD} to 12 V. Then measure V_D and V_R and insert their values in Table 1. Calculate the corresponding value of I_D using Ohm's law. Do the required measurements and calculations for the remaining settings of V_{DD} .

3. Replace the silicon diode with a Zener diode and complete Table 2.

Note: for the negative values of V_{DD} you will need to swap the dc supply leads on the board!

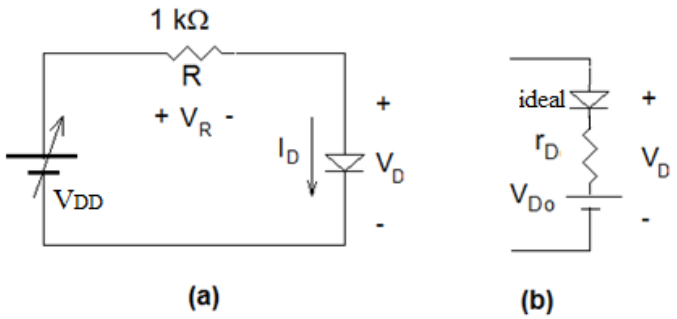


Figure 2 **(a)** Measuring the i-v characteristics. **(b)** A linear model of a forward –biased diode.

2.4 Results

Table 1 **silicon diode** i-v measured data							
V_{DD} (V)	V_R (V)	V_D (V)	$I_D = V_R / R$ (mA)	V_{DD} (V)	V_R (V)	V_D (V)	$I_D = V_R / R$ (mA)
12				-2			
7				-3			
1.5				-3.5			
0.7				-4			
0.5				-4.5			
0.2				-5			
0	0	0	0	-12			

Table 2 **Zener diode** i-v measured data							
V_{DD} (V)	V_R (V)	V_{DZ} (V)	$I_{DZ} = V_R / R$ (mA)	V_{DD} (V)	V_R (V)	V_{DZ} (V)	$I_{DZ} = V_R / R$ (mA)
12				-2			
7				-3			
1.5				-3.5			
0.7				-4			
0.5				-4.5			
0.2				-5			
0	0	0	0	-12			

2.5 Homework

1. Plot I_D vs. V_D for both diodes using MATLAB® (See Appendix A for a code that you may use). Label the three regions of operation.
   Note: You have to print and attach the code as well as the plots.

2. From graph 2, extract a piecewise-linear model in the forward biased region (see Fig. 2b) for the silicon diode, assuming an operating range between (I_{D1} = 1 mA) and (I_{D2} = 10 mA). This can be done as follows:

   i. Find V_{D1} and V_{D2} from your plot (see Fig. 3).

   Using $r_D = (V_{D2} - V_{D1}) / (I_{D2} - I_{D1})$, calculate r_D.

   ii. Calculate V_{Do} as follows:

   $V_{Do} = V_{D1} - I_{D1} \times r_D$ or $V_{Do} = V_{D2} - I_{D2} \times r_D$.

   Alternatively, you can draw a line between these two points and extrapolate it on the V_D axis to find V_{Do} (refer to Fig. 3).

3. For V_{DD} = 7 V, use the piecewise-linear model you have found above to calculate I_D and V_D.
4. For V_{DD} = 7 V, use the load line method to verify the operating point (V_{DQ}, I_{DQ}) by finding its intersection with the measured characteristic curve.
5. Calculate the error % in the V_D obtained in (3) and (4) with respect to the measured value that you have recorded (for V_{DD} = 7 V). Tabulate your results as shown below.
6. Which method is more accurate?

Method	V_D (V)	I_D (mA)	V_D error %
Measured (from Table 1)			0
piecewise-linear model			
curve and load line (graphical method)	V_{DQ} =	I_{DQ} =	

7. Calculate the emission coefficient n for the silicon diode using equation (2) in section 2.2.

V_T = 26 mV at room temperature.

8. Calculate the saturation (also called scale) current I_S of the silicon diode.
9. Propose a dc circuit model for the silicon diode in the reverse bias region ($V_D < 0$).

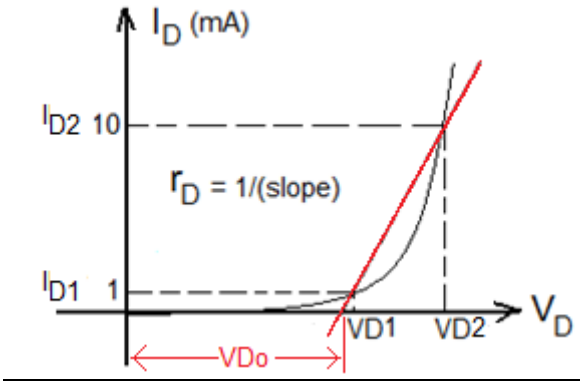


Figure 3 Extracting r_D and V_{Do} from the i-v characteristic.

LAB 3

Diode Applications: The Limiter (Clipper)

3.1 Objective

- To explore the basic principles of some limiter (clipper) circuits.
- To examine their output waveforms and transfer characteristics ($V_O(t)$ vs. $V_i(t)$) on an oscilloscope.
- To be able to design them and predict their transfer characteristics.

3.2 Background

Limiting or clipping is a function performed by a diode network if prevention of the output signal from exceeding or falling below a predetermined voltage level is desired. A diode is suitable for this role because its voltage changes a little for a significant change in its current.

A general voltage transfer characteristic (VTC) of a double limiter is shown in Fig. 1a. The circuit operation can be divided into two regions: linear, where (V_O^-/A_V) < Vi < (V_O^+/A_V), and saturation which extends outside that range. If there is no load connected across its output port, a limiter will have a unity slope in the linear region; i.e., A_V =1.

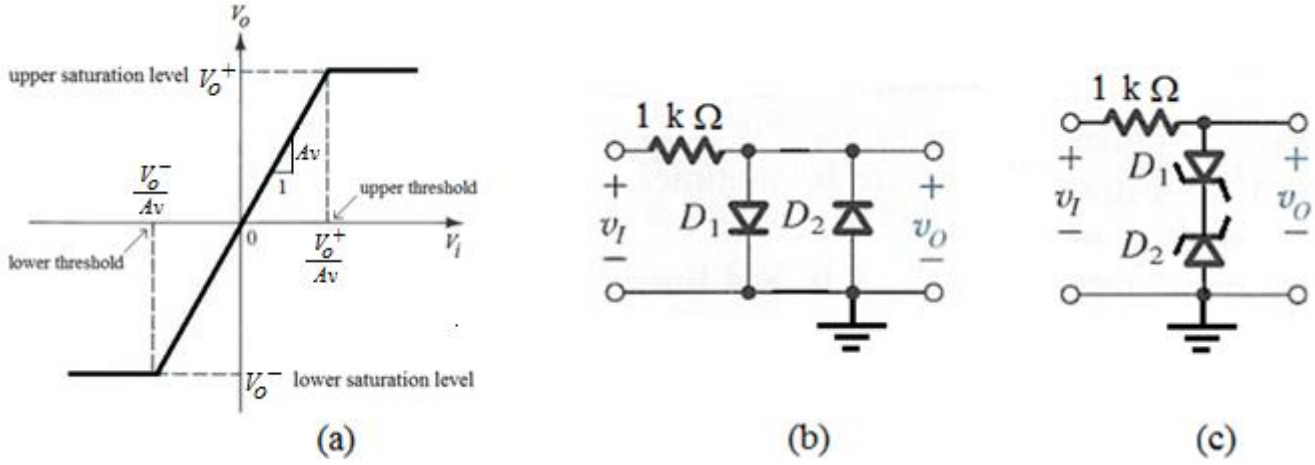
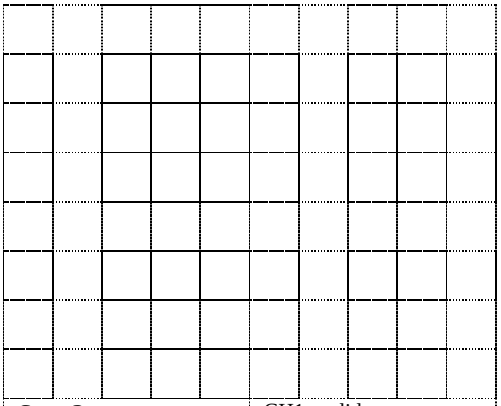


Figure 1 **(a)** VTC of a limiter: **(b)** Two parallel diodes limiter. **(c)** Double-anode Zener limiter.

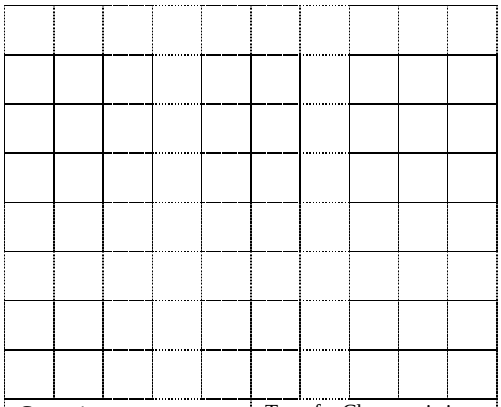
3.3 Procedure

1. Connect the circuit shown in Fig. 1b. Use a sinusoidal input with f = 100 Hz and V_i = 6 $V_{pk\text{-}pk}$.
2. Display $V_i(t)$ on CH1 (**X**) and $V_O(t)$ on CH2 (**Y**) of your oscilloscope. *Use appropriate vertical and horizontal sensitivities and take note of them. Also, use dc coupling on both channels.*
3. Sketch $V_i(t)$and $V_O(t)$ on one grid.
   What happens if D_2 is disconnected?
4. Reconnect D_2. Set your scope on X-Y mode. Set both channels to GND. Adjust the position of the dot-shaped beam to align it at the origin. Set both cannels to dc coupling again. Sketch the circuit's voltage transfer characteristics (VTC).
   What is the upper limiting (saturation) level of the output? What is the upper threshold of the input?
   Effect of loading:
5. Find the above voltages experimentally if a 1-k**Ω** resistor is connected across the output.
   Does the output's upper saturation level change upon loading? How about the input's upper threshold?
6. Increase V_i to 14 $V_{pk\text{-}pk}$ then connect the circuit shown in Fig. 1c. Redo step (3) then (4)—No need to disconnect D_2.
   Determine the upper limiting (saturation) level of the output; i.e., V_O^+.
   What is the expected value of V_O^+ in terms of V_Z (assuming 0.7-V-drop model in forward)? Calculate V_Z.

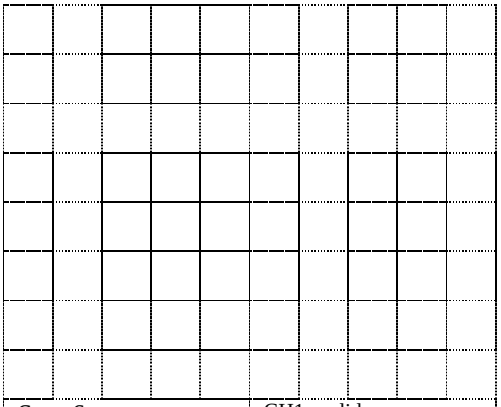
3.4 Results



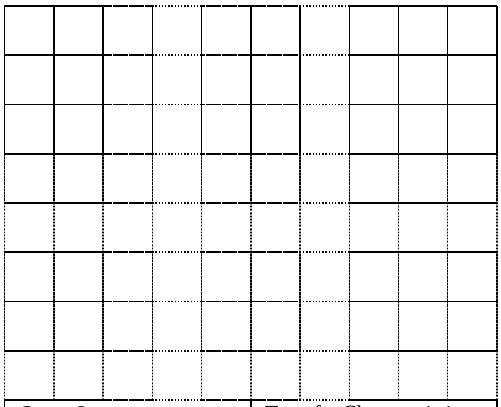
Step 3	CH1 solid —— CH2 dotted ------
CH1 (V/DIV) :	CH2 (V/DIV) :



Step 4	Transfer Characteristics
CH1 (V/DIV) :	CH2 (V/DIV) :



Step 6	CH1 solid —— CH2 dotted ------
CH1 (V/DIV) :	CH2 (V/DIV) :



Step 6	Transfer Characteristics
CH1 (V/DIV) :	CH2 (V/DIV) :

Use the questions in the above procedure (section 3.3) as a guide to write a conclusion.

3.5 Homework

1. Design a circuit that implements a transfer characteristic like the one shown in Fig. 2a. *Use the 0.7-V-drop model for a forward-biased silicon diode.*

2. For the circuit shown in Fig .2b, sketch its *expected* transfer characteristic.

3. Assume that a sinusoidal input of 10-V peak amplitude (20 $V_{pk\text{-}pk}$) is applied to the circuit shown in Fig. 2b. Sketch the *expected* output voltage waveform; For a Zener diode, use *a 0.7-V-drop model in the forward-bias region and a constant-voltage-drop model of* V_Z *in the breakdown region.*

4. Repeat this question in case of a 4-V peak amplitude input.

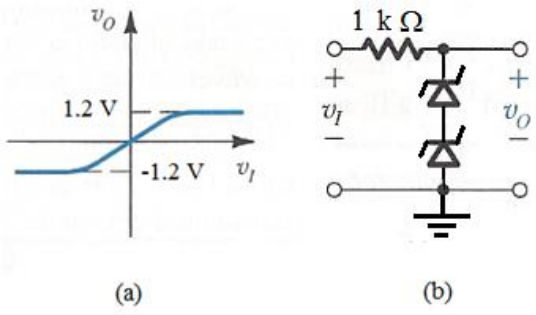


Figure 2

LAB 4

Diode Applications: ac to dc Conversion

4.1 Objective

- The main aim of this experiment is to introduce the student to an important application of diodes, namely the process of ac to dc conversion.
  This task will hopefully achieved by studying a simple *unregulated* dc power supply, which is essentially a rectifier followed by a low-pass filter.

4.2 Background

dc power supplies are essential part of electronic equipment. A block diagram of such a system is shown in Fig. 1. This system involves rectification, filtering and voltage regulation.

A transformer is used to step down the input ac voltage and provide electrical isolation (important for safety). A diode rectifier uses the unidirectional-current property of diodes to convert an input sinusoid to a unipolar but pulsating output. Acting as a simple low-pass filter, a capacitor is used to reduce the pulsation (ripple) of the resulting output.

However, the ripple would be inversely proportional to C and R_L. So, a voltage regulator is used to regulate the dc output voltage against load and/or ac input variations. We shall examine the effect and benefits of voltage regulation in lab 5.

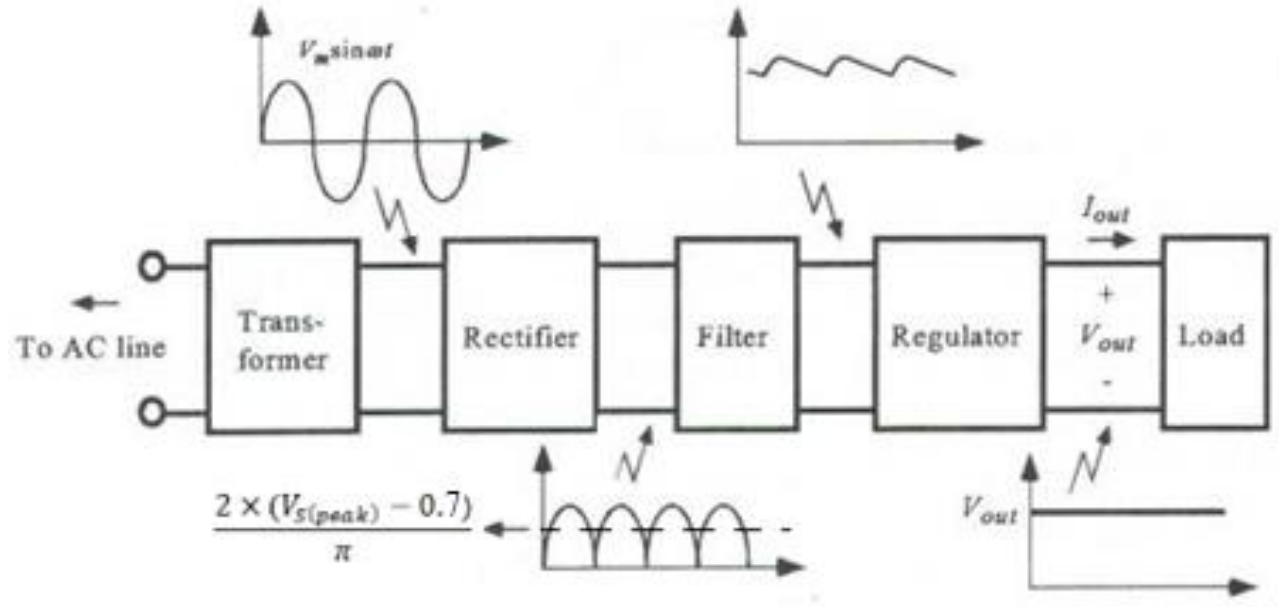


Figure 1 A block diagram of a dc power supply.

4.3 Procedure

Half-Wave Rectifier:

1. Connect the circuit shown in Fig. 2a. Use two oscilloscope probes to display $V_S(t)$ on channel I (**X**) and $V_O(t)$ on channel II (**Y**). Set both channels of your oscilloscope to *setting 1* (Table 1). Display both waveforms at the same time by setting the scope on DUAL display mode. Record the two waveforms on the same graph. Measure and record the average value of $V_O(t)$ using a digital multimeter set to measure dc volts.

Full-Wave Rectifier:

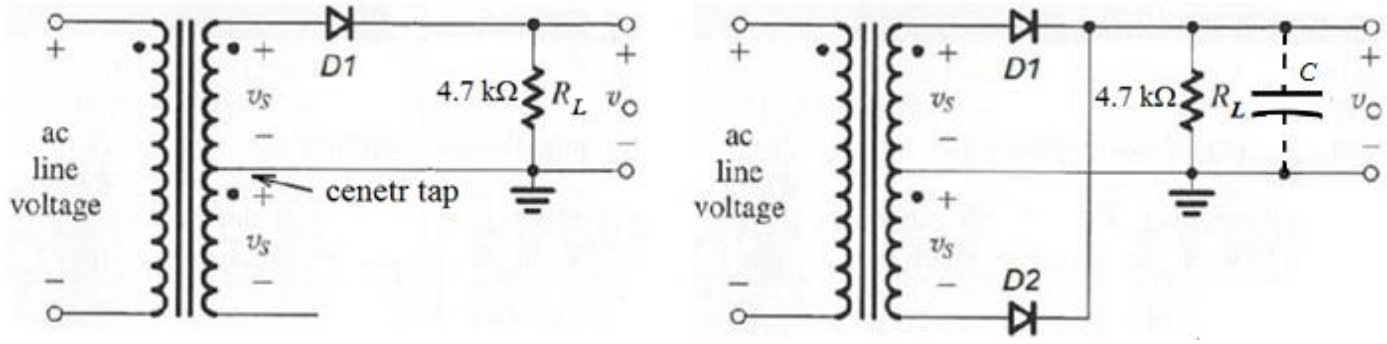
2. Connect D_2 as shown in Fig. 2b. Display and record $V_S(t)$ and $V_O(t)$ on the same graph. Measure the average value of $V_O(t)$ by a digital multimeter. *Why does the average value of $V_O(t)$ increase when we use two diodes instead of two?*

Effect of output voltage filtering:

3. Set CH2 of your scope to *setting 2*. Connect a 10-µF electrolytic capacitor (with negative lead connected to ground) in parallel with R_L. Display and record $V_O(t)$.
4. Replace the 10-µF capacitor with a 470-µF one. Display and record $V_O(t)$. *How does increasing C affect the output ripple?*

Effect of reducing R_L:

5. Replace the 4.7-kΩ with a 270-Ω one. Note how the ripple changes. *How does that affect the output ripple? Is this good or bad?*



(a) (b)

Figure 2 Rectifier using a center-tapped transformer: **(a)** half-wave; **(b)** full-wave.

Table 1: Scope Settings					
Setting	Vertical Sensitivity VOLT/DIV	Horizontal Sensitivity mS/DIV	Coupling	Ground Level Position	Trigger
1	5	5	dc	center	Line (ac)
2	2	5	dc	bottom	Line (ac)

4.4 Results

Step 1: $V_O(DC) =$	$V_S(t)$ _____ $V_O(t)$ ------
Half-Wave Rectifier	

Step 2 $V_O(DC) =$	$V_S(t)$ _____ $V_O(t)$ ------
Full-Wave Rectifier	

Step 3 Record Only $V_O(t)$	C_L = 10 µF R_L = 4.7 kΩ
Poorly Filtered Full-Wave Rectifier	

Step 4 Record Only $V_O(t)$	C_L = 470 µF R_L = 4.7 kΩ
Appropriately Filtered Full-Wave Rectifier	

Step 5 Record Only $V_O(t)$	C_L = 470 µF R_L = 270 Ω
Effect of Reducing R_L	

4.5 Homework

1) Write down a conclusion that reflects your observations and understanding of the objectives of this experiment.

2) In the full-wave rectifier circuit, what is your observation regarding direction of the current that flows in R_L during a complete cycle of the output waveform?

3) In the full-wave rectifier circuit, what is the peak value of $V_S(t)$? What is the maximum current that a conducting diode must be able to handle if R_L = 1 kΩ.

4) The **p**eak **i**nverse **v**oltage (PIV) rating of a diode is the maximum voltage it can withstand without breakdown. Find out a suitable PIV rating of D_1 and D_2 in the full-wave rectifier with 50% safety margin.

Hint: write a loop equation to find the maximum voltage across a reverse biased diode then select a PIV of 1.5 times that value.

LAB 5

Computer Simulation of Electronic Circuits

5.1 Objective

In this lab, you will be introduced to computer simulation of electronic circuits. Specifically, you will use the free Lite Demo version of OrCAD (Capture & PSpice) to draw and simulate some simple circuits.

5.2 Background

OrCAD (Capture & PSpice) is a version of SPICE (Simulation Program for Integrated Circuit Engineering). SPICE was developed at the University of California at Berkeley in the 1970s, and has been the most widely used circuit simulator in the electronics industry. The required steps to using OrCAD (Capture & PSpice) can be summarized as follows:

1) Draw an electronic circuit on the computer using Capture.
2) Setting an appropriate simulation profile that includes analysis types like: bias point, dc sweep, ac sweep and time domain.
3) Running PSpice from within Capture to obtain the results/plots of the chosen analysis in step 2.

A good introduction to OrCAD (Capture & PSpice) can be found here:

http://userweb.eng.gla.ac.uk/john.davies/orcad/spiceintro160.pdf

The latest version of the OrCAD Lite Demo software (Capture & PSpice) can be downloaded via the following link:

http://www.orcad.com/resources/orcad-downloads

5.3 Regulated Power Supply:

1. Double click the OrCAD Capture icon on the desktop.
2. Go to File ⇨ New Project. Your project should be named: ckt2_xxxx, where xxxx stands for the last four digits of your student number. Keep the first choice selected. In the second window select: Create a blank project then click OK.
3. First, you have to add all of the needed parts on the workarea. You may do that either by clicking on the ***Place part*** icon on the right-hand toolbar or simply typing **p**. The parts to be added are: VSIN/SOURCE, R/ANALOG, D1N4002/EVAL (4),
4. Wire all the parts as shown in Fig. 1a. You may do that either by clicking on the ***Place wire*** icon on the right-hand toolbar or simply typing **w**.
5. Ground your circuit where needed. You may do that either by clicking on the ***Place ground*** icon on the right-hand toolbar or simply typing **g**; use the 0/CAPSYM type of ground.

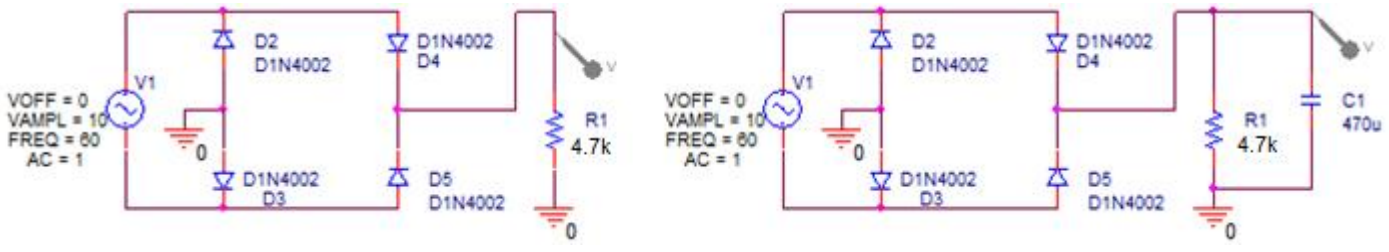


Figure 1 Bridge rectifier **(a)** without filtering and **(b)** with filtering.

6. Double click on each V1 parameter and set it at the value shown in the Fig. 1a.
7. From PSpice (top menu), select: New Simulation Profile. Name it for example: dc_sweep. Set analysis type at: dc Sweep. Set the sweep variable to V_1. Start from -10 and end at 10 with an increment of [10-(-10)]/1000 = 20m.
8. Place a voltage/level marker on top of the R_1 to display the transfer characteristic of the circuit.
9. Run your simulation and examine characteristic. What mathematical function does it look like?
10. From PSpice (top menu), select: New Simulation Profile. Name it for example: time_domain. Set analysis type at: Time Domain (transient). Start from 0 up to 50ms (3 cycles of our 60-Hz input) with a maximum step size of 50ms/1000 = 50us.
11. Place a **differential voltage marker** across the input.
12. Run your simulation and examine the input and output voltage waveforms. *Does the output waveform look familiar to you? What does this circuit do?*
13. Connect the capacitor as shown in Fig 1b and rerun the simulation to see how that affects the ripple in the output voltage waveform.
14. Decease the value of R_1 to 270 Ω and rerun to see how that affects the ripple in the output.
15. Add a voltage regulator to your dc supply circuit as shown in Fig. 2. Change R_1 back to 4.7 kΩ. Rerun the simulation. *What does the output waveform look like? How is the output voltage level related to V_Z of the Zener diode?*
16. Reduce R_1 to 270 Ω and rerun to see how that affects the ripple in the output.

What is your conclusion about the importance of the voltage regulator?

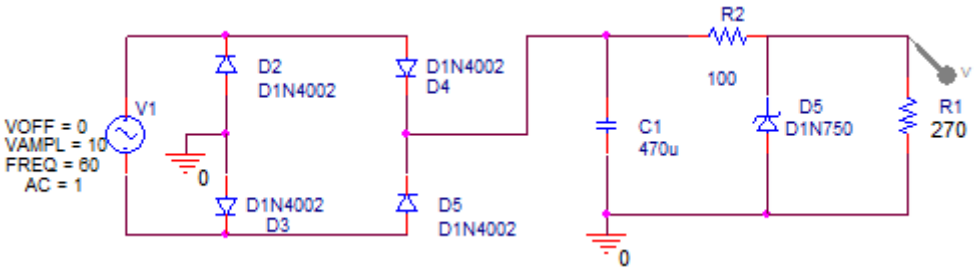


Figure 2 Regulated power supply.

5.4 Clipper Circuit (Homework):

1. Using an appropriate number of D1N4002 diodes, design and simulate a clipper circuit that limits its output approximately between 2.8 V and -1.4 V (Figure 3).
2. Double click the OrCAD Capture icon on the desktop.
3. Go to File ⇨ New Project. Your project should be named: ckt2_xxxx, where xxxx stands for the last four digits of your student number. Keep the first choice selected. In the second window select: create a blank project then click OK.
4. Draw the circuit that you have designed in setp1.
5. For the input source V_1, use a (VSIN) part with 4-V peak ude, 1-kHz frequency and a zero offset.
6. From PSpice (top menu), select: New Simulation Profile. Name it for example: time_domain. Set analysis type at: Time Domain. Start from 0 up to 3 ms with appropriate maximum step size.
7. Place a voltage/level marker on top of V_1 and across the output (on top of D_1).
8. Run your simulation to display $v_i(t)$ and $v_o(t)$.
9. From PSpice (top menu), select: New Simulation Profile. Name it for example: dc_sweep. Set analysis type at dc Sweep. Sweep V_1 from -4 to 4V with appropriate increment.
10. Click on the input voltage/level marker and hit delete on the keyboard.
11. Run your circuit to see its transfer characteristic.
12. Print and submit :
    - The circuit diagram (with your name typed on lower right corner)
    - $v_i(t)$ and $v_o(t)$.
    - The transfer characteristic.
    - From your plots, find the upper and lower saturation levels to verify that they meet the specifications.

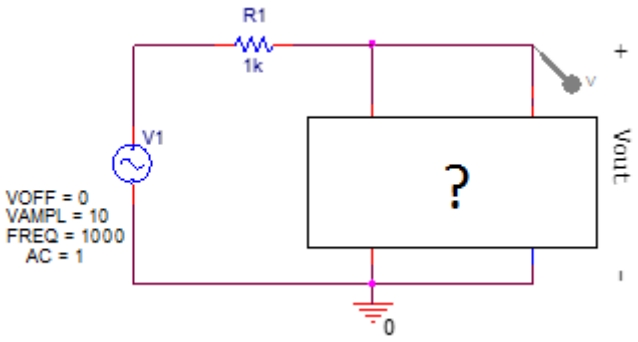


Figure 3

LAB 6

An Introduction to the Operational Amplifier

6.1 Objective

To get acquainted with the operational amplifier (op amp) through two of its applications: a noninverting amplifier and a comparator to sense light intensity change.

6.2 Background

The op amp is a versatile *integrated circuit* (IC) that perform various types of analog signal processing tasks. The most popular op amp is the μA 741 which was introduced by Fairchild in 1968 to become the industry standard. Its pinout is shown in Figure 1.

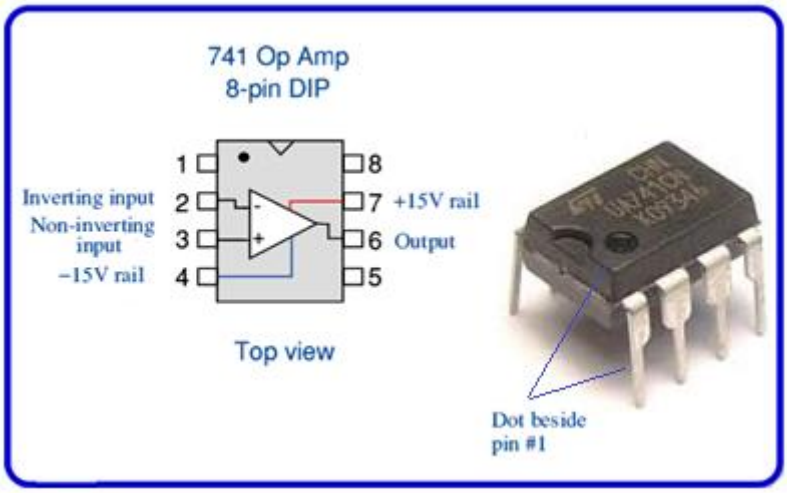


Figure 1 The popular μA 741 op amp IC package and its pinout.

An op amp *amplifies the difference* between two input voltages and produces a *single output*. It is characterized a very large open-loop gain (A), a very large input impedance, and a very small output impedance. Stable closed-loop gains can be obtained using negative feedback. For a noninverting configuration (Fig. 2(a)), the closed-loop gain (G) can is ideally given by:

$$G \equiv \frac{v_o}{v_i} = 1 + \frac{R2}{R1} \qquad (1)$$

A photocell (also called photoresistor or light dependent resistor, LDR) is a resistor whose resistance (R_{cell}) decreases with increasing incident light intensity. It is made of a high resistance semiconductor such as cadmium sulfide (CdS). We shall use such a resistor along with an op-amp connected in an open-loop configuration (to work as a comparator) to detect changes in light intensity (Fig. 2(b)).

For that circuit, and since the op amp draws negligible current, V_P and V_N (with respect to ground) can be found by the voltage divider rule:

$$V_P = [(15) - (-15)] \times \left(\frac{R3}{Rcell+R3}\right) + (-15) \qquad (2.a)$$

$$V_N = [(15) - (-15)] \times \left(\frac{R2}{R2+R1}\right) + (-15) \qquad (2.b)$$

For low values of R_{cell} (uncovered): $V_P > V_N \rightarrow V_O \approx 13.5$ V,

For high values of R_{cell} (covered) : $V_P < V_N \rightarrow V_O \approx -13.5$ V.

6.3.1 Procedure A: Noninverting Amplifier

1. Connect the circuit shown in Fig. 1a. Set your input sinusoidal at 1 V (peak to peak) and a frequency of 1 kHz. Start with R_2 of 10 kΩ. Display and sketch $v_i(t)$ *and* $v_O(t)$.
2. Measure and record the peak-to-peak value of the output and determine the closed-loop gain using:

$$G = \frac{V_{o(\text{pk-pk})}}{V_{i(\text{pk-pk})}} \quad (3)$$

3. Change R_2 to 39 kΩ ; display and sketch $v_i(t)$ *and* $v_O(t)$.

6.3.2 Procedure B: Detecting Light Intensity Change

1. Measure the resitance of a covered and uncovered photocell by a multimeter and record that in Table 2.
2. Connect the circuit shown in Fig. 1b. Using a DMM, measure V_P, V_N, and V_O (with respect to the COM). *Which LED glows? Record your findings in Table 2.*
3. Cover the photocell (LDR) and repeat the previous step.

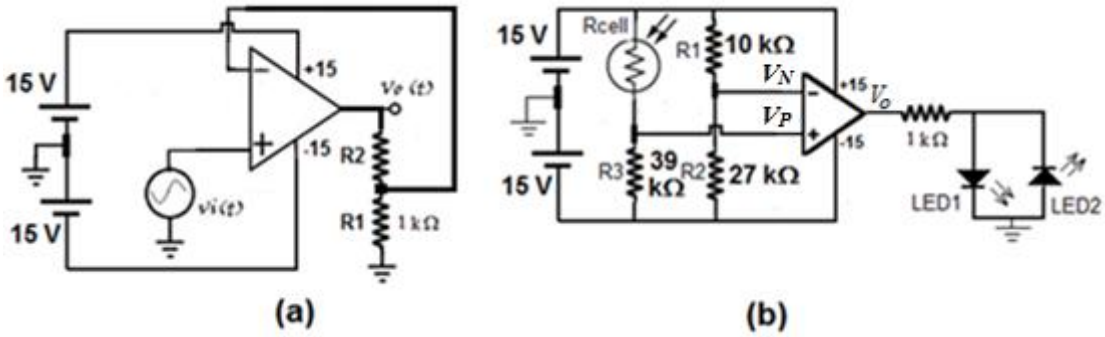
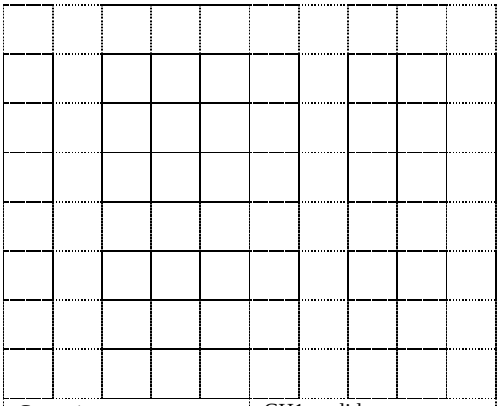
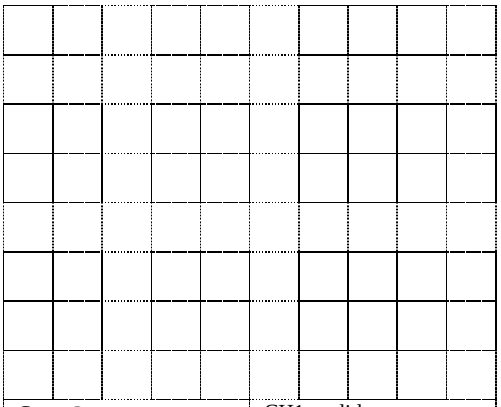


Figure 1 Op amp circuits: **(a)** noninverting amplifier **(b)** comparator to sense light intensity change.

5.4 Results



Step 1	CH1 solid —— CH2 dotted ------
CH1 (V/DIV):	CH2 (V/DIV):



Step 2	CH1 solid —— CH2 dotted ------
CH1 (V/DIV):	CH2 (V/DIV):

Table 1			
R_2 value	*Vo*(peak-peak)	Measued Gain = $V_{o(pk\text{-}pk)} / V_{i(pk\text{-}pk)}$	Theoritical Gain (eqn 1)
10 kΩ			
39 kΩ		xxxxxxxxxxxxxxxxx Undefined; output clipped	

Table 2				
R_{cell} (uncovered):		R_{cell} (covered):		
case	V_P	V_N	V_O	which LED glows?
uncovered				
covered				

6.5 Homework

1. In step 1 of procedure A, comment on the phase shift between $v_i(t)\ and\ v_O(t)$.

2. In step 2 of procedure A, what has happened to the shape of $v_O(t)$? Why?

3. Calculate the maximum value of R_2 which will produce unclipped output for an input of 1 $V_{pk\text{-}pk}$.

4. In both cases of procedure B, indicate whether the op amp is sourcing or sinking current.

5. Think of a way to switch on LED2 at darker conditions.

LAB 7

N-MOSFET i_D-v_{DS} Characteristics

7.1 Objective

To introduce the student to the MOSFET (Metal Oxide Semiconductor Field Effect Transistor,) examine its i-v characteristics and measure some of its important parameters. The MOSFET that will be used in this experiment is the IRF620.

7.2 Background

The MOSFET is a three-terminal device that is used mainly as an electronic switch (in triode and cutoff modes of operation) or as an amplifier (in saturation mode.) Saturation mode is characterized by a weak dependence of i_D on v_{DS} and a much greater dependence on v_{GS}.

The value of v_{GS} at which a conducting channel between the drain and the source is induced is called the threshold voltage, V_t.

To act as a good amplifier, a MOSFET has to have a high transconducatnce, g_m; it reflects how much the drain current will change for a small change in v_{GS} in the saturation region at a constant v_{DS}.

7.3.1 Procedure A: Threshold Voltage Measurement

1. Connect the circuit shown in Fig. 1a.
2. Increase V_{DD} until V_{1k} becomes 0.25V (250 mV).
3. At that point, measure and record the value of V_{GS} using a dc voltmeter.
   This value of V_{GS} will approximately be equal to the threshold voltage, V_t.

Threshold voltage (V_t) = ……

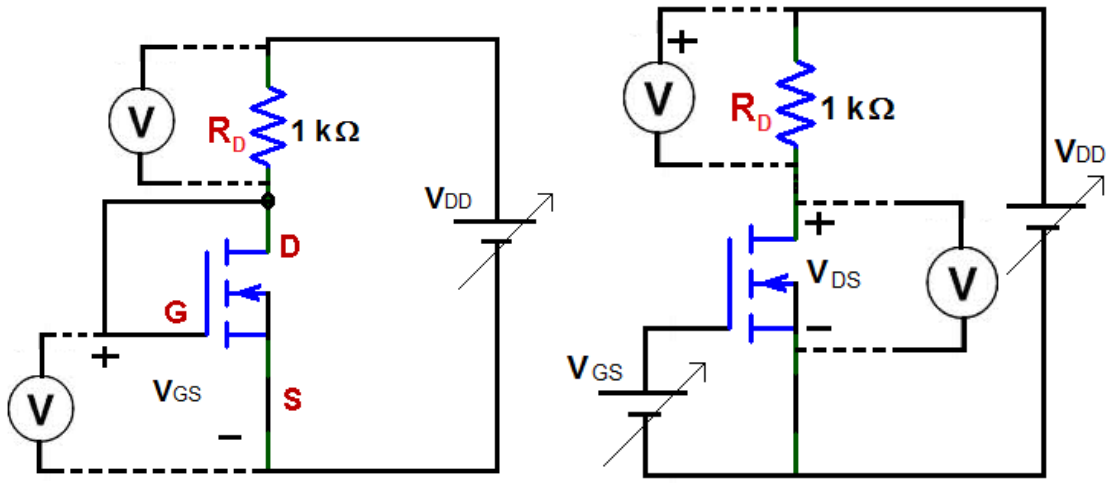
7.3.2 Procedure B: Output (Drain) Characteristics Measurement

1. Connect the circuit shown in Fig. 1b.
2. Set V_{GS} at (Vt + 0.1 = V_{GS1}); V_t being as measured in procedure A. *Verify this value using a voltmeter.*
3. Vary V_{DD} to obtain the V_{DS} values shown in Table 1. For each value of V_{DS}, measure and record V_{RD}. *The corresponding values of I_D can be found from Ohm's law.*

4. Increase V_{GS} by 0.1 V, that is V_{GS2} = Vt + 0.2; *verify this value using a voltmeter*. Redo step 3.
5. Increase V_{GS} by 0.1 V, that is V_{GS3} = Vt + 0.3; *verify this value using a voltmeter*. Redo step 3.
6. Increase V_{GS} by 0.01 V, that is V_{GS4} = Vt + 0.31 while keeping V_{DS} at 2 V . Measure and record I_D.

7.4 Results

Table 1									
V_{GS1} = V_t + 0.1 V			V_{GS2} = V_t + 0.2 V			V_{GS3} = V_t + 0.3 V			
V_{DS} (V)	V_{RD} (V)	I_D (mA)	V_{DS} (V)	V_{RD} (V)	I_D (mA)	V_{DS} (V)	V_{RD} (V)	I_D (mA)	
0	0	0	0	0	0	0	0	0	
.02			.02			.02			
.05			.05			.05			
0.1			0.1			0.1			
0.2			0.2			0.2			
0.3			0.3			0.3			
0.5			0.5			0.5			
2			2			2			I_D @ V_{GS4} and V_{DS} = 2V



(a) (b)

Figure 1 Circuit setup for measuring: **(a)** the threshold voltage, **(b)** the i_D-v_{DS} characteristics.

7.5 Homework

1. Use MATLAB® (See Appendix A) to plot i_D (mA) vs. v_{DS} (V) for each value of v_{GS}. Label each curve with the corresponding values of v_{GS}.
   Also, mark $V_{DS(sat)} = V_{GS} - V_t = V_{OV}$ for each curve.
2. What is the shape of the relationship between i_D and v_{OV}? Label the three regions of operation on your graph (cutoff, triode, saturation).
3. Calculate ($k'_n \frac{w}{L}$) for this MOSFET using any pair of measurements (v_{GS} and i_D) in saturation.
4. From step 6 of procedure B, calculate g_m which, in saturation, is defined as: $g_m = \frac{\Delta i_D}{\Delta v_{GS}}\Big|_{\substack{\text{constant} \\ \text{VDS}}}$.
5. Verify that value using: $g_m = \frac{2I_D}{V_{GS} - V_t}$. Compare the two values of g_m and comment.
6. In saturation, how does i_D change with v_{DS}?
7. Calculate r_o for V_{OV} = 0.3 V.
8. Calculate the intrinsic voltage gain $A_o = g_m r_o$ of this MOSFET for V_{OV} = 0.3 V.

LAB 8

VTC and Large Signal Operation of the CS Circuit

8.1 Objective

To experimentally obtain and examine the voltage transfer characteristic (VTC) of the common-source circuit and learn its implications on using that circuit as a common-source amplifier or as a passive-load inverter.

8.2 Background

A great deal of information can be learned for a specific circuit by studying its VTC.

For example, the region characterized by a high gain can be utilized for voltage amplification. In contrast, regions characterized by maximum or minimum output voltage levels may be taken advantage of in switching application like logic gates.

If a square wave is applied to the input of the common-source circuit, it acts as a logic inverter. An inverter loaded with capacitance will respond sluggishly due to RC delay caused by the requirement to charge and discharge the capacitive load.

8.3.1 Procedure A: VTC for the Common Source Circuit

1. Connect the circuit shown in Fig. 1a.
2. Set your scope at X-Y mode. Connect your input to CH1 (X) and your output to CH2 (Y). Set the vertical sensitivity of each channel at 1 V/DIV.
3. Use a decade box to set R_D at 470 Ω then at 10 kΩ. Sketch the transfer characteristics for each case on the the graph of Fig. 2.

8.3.2 Procedure B: Large Signal Operation: the passive-load Inverter

4. Readjust R_D to 10 kΩ and use the TTL output of your signal generator to apply a square wave to CS circuit. Sketch the input and the output as they appear on the scope. Position the two signals on top of each other (their GND levels should be separate in order to identify them clearly).
5. Connect a 10-nF loading capacitor (C_L) between the output node and ground. Record the output waveform.
6. Replace the 10-nF capacitor with a 100-nF one. Record the output waveform.

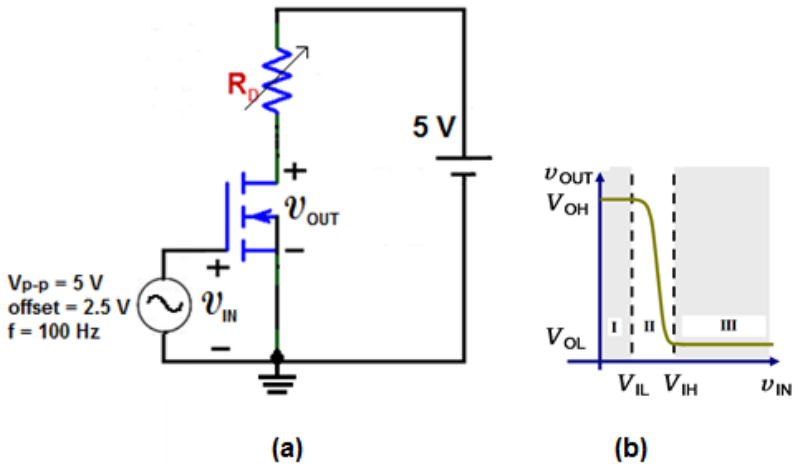


Figure 1 **(a)** The common-source circuit; **(b)** Its VTC.

8.4 Results

Figure 2 VTC for the CS circuit

Procedure B Step 1	CH1 solid —— CH2 dotted ------
CH1 (V/DIV):	CH2 (V/DIV):

Procedure B Step 2, 3	C_L=10 nF solid — C_L=100 nF dotted ----
CH1 (V/DIV):	CH2 (V/DIV):

8.5 Homework

1. In procedure A:
   a. Label the VTC you have obtained with the three regions (modes) of operation of the MOSFET.
   b. For R_D = 470 Ω, what is the value of dc offset required to operate this circuit as an amplifier?

   c. How is the voltage gain A_V related to the slope of the VTC? Which value of R_D corresponds to a higher *magnitude* of A_V? Why?

2. In procedure B:
   a. The rise time of a waveform, t_r, is the time it takes to increase from 10% to 90% of its final value. How does a capacitive load affect t_r of V_{out}?
   b. Examine the waveform of step 6, then compare the rise time of the output waveform to its fall time. Which is smaller? Why?

   c. If the input alternates between 0 and 5 V, the bias point Q of the MOSFET alternates between…… and…… modes of operation.

LAB 9

VTC of the Common-Emitter Circuit

9.1 Objective

To introduce the student to the *npn* Bipolar Junction Transistor (BJT) by studying the voltage transfer characteristic (VTC) of a simple common-emitter (grounded emitter) circuit.

9.2 Background

The BJT is a three terminal device that find uses in automotive applications, radio frequency (RF) circuits, and very high-speed digital circuits.

Its three terminals are connected to three semiconductor layers: the emitter, the base, and the collector. As such, it consists of two *pn* junctions, the emitter-base junction (EBJ) and the collector-base junction (CBJ). Based on the bias condition of these two junctions, three distinct modes of operation are obtained, as shown in Table 1 for an *npn* transistor.

The **cutoff mode** and the **saturation mode** are employed in switching applications (e.g., logic circuits). The **active mode** is the one used if the transistor is to operate as an amplifier.

Table 1		
mode	EBJ bias condition	CBJ bias condition
Cutoff	$v_{BE} < V_{BE\,on} \approx 0.5$ V $\Rightarrow$ reverse/slightly-forward	$v_{BC} < V_{BC\,on} \approx 0.4$ V $\Rightarrow$ reverse/slightly-forward
Active	$v_{BE} \geq V_{BE\,on} \approx 0.5$ V $\Rightarrow$ forward	$v_{BC} \leq V_{BC\,on} \approx 0.4$ V $\Rightarrow$ reverse/slightly-forward
Saturation	$v_{BE} \geq V_{BE\,on} \approx 0.5$ V $\Rightarrow$ forward	$v_{BC} > V_{BC\,on} \approx 0.4$ V $\Rightarrow$ forward
General Relationships: $I_E = I_B + I_C$		$V_{BC} = V_{BE} - V_{CE}$
In the **active** mode: $v_{CE} > 0.2$ V ; $\beta \equiv I_C / I_B$; $\alpha \equiv I_C / I_E$; $\alpha = \beta / (\beta+1)$		
In the **saturation** mode: $v_{CE} = V_{CE\,sat} = 0.1 - 0.2$ V ; $\beta_{forced} \equiv I_{Csat} / I_B$		

For the CE circuit shown in Fig. 1,

$I_B = (V_{IN} - V_{BE})/R_B$ (1) and $I_C = (V_{CC} - V_{out}) / R_C$ (2)

9.3 Procedure

1. Connect the circuit shown in Fig. 1. Fix V_{CC} at 5 V and vary V_{IN} to obtain the V_{OUT} values shown in Table 1. For each value of V_{OUT} measure V_{BE} and V_{IN}.
2. Do the required calculations in Table 1 using the relevant equations given in section 9.2.

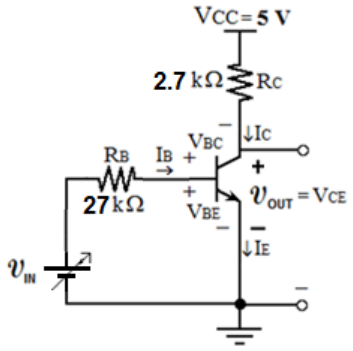


Figure 1 The Common Emitter Circuit.

9.4 Results

Table 1 (Use 3 decimal digits to record V_{IN} and V_{BE}.)						
Measurements			Calculations			
V_{IN} (V)	V_{BE} (V)	$V_{CE} = V_{OUT}$ (V)	$V_{BC} = V_{BE} - V_{CE}$ (V)	Mode of operation	I_B (mA)	I_C (mA)
0.000	0.000	5.00	-5	Cutoff	0	0
		4.95				
		4.50				
		4.00				
		3.00				
		2.00				
		1.00				
		0.30				
		0.20				
		0.10				

Figure 2 VTC of the CE circuit.

9.5 Homework

1. Plot the dc transfer characteristic ($v_{OUT}\ vs.\ v_{IN}$) on the graph of Fig. 2.
2. Label the three modes of operation on the graph.

3. Which region of the above characteristic can be used for voltage amplification? Why?

4. Calculate β at v_{OUT} = 2.5 V. Also, calculate $\beta_{forced} \equiv I_{Csat} / I_B$, at v_{OUT} = 0.1 V. Compare the two values.

5. As the operating point of the BJT moves into saturation, which current begins to saturate I_E, I_B or I_C?

6. Calculate the voltage gains $G_V = \Delta v_{OUT} / \Delta v_{IN}$ and $A_V = \Delta v_{OUT} / \Delta v_{BE}$ when v_{OUT} changes from 3.0 to 2.5 V. Why is A_V usually less than G_V ?

LAB 10

The Common Emitter Amplifier

10.1 Objective

To explore an important application of the BJT, namely using it to amplify a small signal. Specifically, a common (grounded) emitter amplifier will be examined from the dc and small signal perspective.

10.2 Background

The Common Emitter (CE) amplifier is the most famous of the three BJT amplifier configurations. The other two being the common base (used to achieve higher bandwidth) and the common collector (used as a voltage buffer to drive low-impedance loads). The CE amplifier receives the input signal at the base (via a coupling capacitor) and delivers the output from the collector.

Figure 1a shows only the dc circuit of such an amplifier. The dc bias scheme used here is known as the voltage divider bias with emitter degeneration resistance R_E. It is highly desirable to select the values of the bias resistors in such a way to make the operating point $Q = Q(I_C, V_{CE})$ relatively independent of $V_{BE(on)}$ and β which vary with temperature and across samples of a given transistor type.

Starting with a $V_{BE(on)}$ of 0.7 V and a β of 100 as nominal values, for a given I_E (based on power budget) a proposed sizing scheme of the resistors goes like this:

- Start with $V_E = (1/3)\ V_{CC} \Rightarrow$ calculate R_E from Ohm's law $\Rightarrow$ select $R_C = R_E$ ($I_C \approx I_E$).
- Calculate $V_B = (1/3)\ V_{CC} + 0.7$ and $I_B = I_E/(\beta+1) \Rightarrow$ Take I_{R2} to be at least $10I_B \Rightarrow$ calculate R_2 from Ohm's law.
- Given that $I_{R1} \approx I_{R2}$ (why?), calculate R_1 from Ohm's law.

Figure 1b shows the complete CE amplifier circuit. An emitter degeneration resistance, R_E, is used to stabilize the dc bias point (or quiescent point, Q) against variations in β. Moreover, including R_E increases the amplifier's input impedance, and increases its linear range. However, it turns out that R_E has a negative impact on the voltage gain. This effect can be remedied by using a bypass capacitor, C_E, to bypass R_E at signal frequencies. Coupling capacitors, C_1 and C_2 are used to act as short circuits at signal frequencies of interests while blocking dc. The CE amplifier is characterized by a 180° phase difference between its input and ouput voltages. It's an indication of the inverse relationship (negative slope) between its input and output voltages as you may recall from lab 9.

The theoretical no-load voltage gain A_V of the CE amplifier with an efficiently bypassed R_E is given by the following expressions:

$$A_V = -g_m(R_C \parallel r_o)$$

$$A_V \approx -g_m R_C \qquad \text{if } R_C \ll r_o$$

$$A_V \approx -\alpha\frac{R_C}{r_e} \approx -\frac{R_C}{r_e} \qquad (1)$$

where

$$r_e = \frac{V_T}{I_E} \qquad (V_T = 26 \text{ mV at room temperature})$$

10.3.1 Procedure A: dc Measurements

1. Measure each resistor by a DMM and record its value in the table given below.
2. Connect the circuit shown in Fig. 1a.
3. Measure and record the values of V_{BE}, V_{BC}, V_{R1}, V_{R2}, V_{RC} and V_{RE} on Fig. 2.
4. Indicate the mode of operation (cutoff, saturation or active) based on V_{BE} and V_{BC}.
5. Using Ohm's law, calculate I_C, I_E, I_{R1} and I_{R2}. Show their values and direction on Fig. 2.
6. Using a node equation, calculate I_B. Show its value and direction on Fig. 2.
7. Calculate and record $\beta = I_C / I_B$ and $\alpha = \beta/(\beta + 1)$.
8. Calculate the theoretical voltage gain A_V given by equation (1).

10.3.2 Procedure B: Small Signal Measurements

1. Connect the circuit shown in Fig 1.(b), initially without C_E.
2. Using a signal generator, apply to your circuit a 20-$mV_{pk\text{-}pk}$, 1-kHz sinusoid.
3. Display and sketch $v_i(t)$ and $v_O(t)$. What is the phase difference between these two signals?
4. Measure $V_{o\ (pk\text{-}pk)}$ and calculate the voltage gain: $A_V = V_{o\ (pk\text{-}pk)} / V_{i\ (pk\text{-}pk)}$.
5. Re-measure A_V with C_E connected (no need to sketch $v_O(t)$ in this case).
6. Increase $V_{i\ (pk\text{-}pk)}$ to 500 mV; set the scope on dc coupling and 2V/DIV; display and sketch $v_C(t)$.

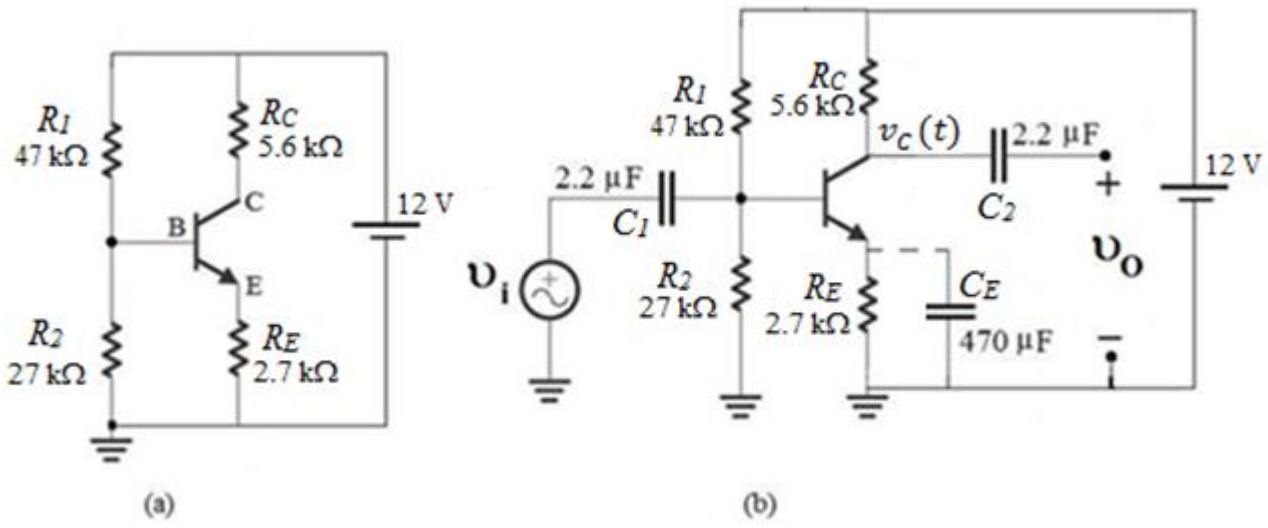


Figure 1 (a) The CE amplifier circuit to measure the dc voltages and currents. **(b)** The complete amplifier.

10.4 Results

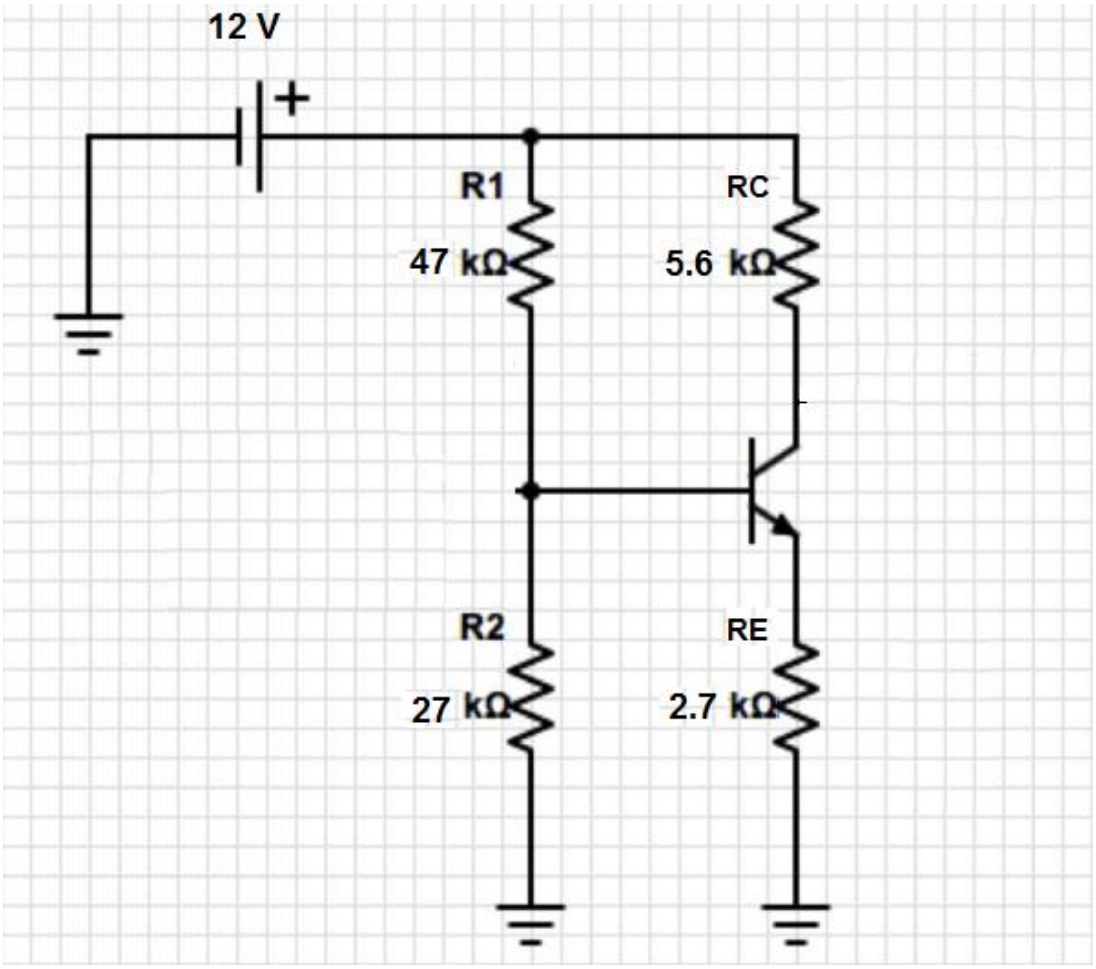


Figure 2

Step 3, 4 and 5	CH1 solid —— CH2 dotted ------
CH1 (V/DIV): CH2 (V/DIV):	A_v (step 3)= Phase shift = A_v (step 5)=

Step 6	CH1 solid —— CH2 dotted ------
CH1 (V/DIV): CH2 (V/DIV):	Comment:

10.5 Homework

1. Assuming V_{CC} = 15, $V_{BE(on)}$ = 0.7 V and a β = 100 in the circuit of Fig. 1a, specify standard 5% resistors (see appendix E) to bias the BJT at I_E = 3 mA.

2. What is the role of R_E and how does it affect the voltage gain, A_V? How can we counteract this effect at signal frequencies?

3. What are the roles of C_1, C_2?

4. In step 6 of procedure B, what has happened to the output? Why? Label the maximum and minimum $v_C(t)$ levels with the appropriate modes of operation.

Appendix A

MATLAB® Code

(LAB 2)

```
clf
% store voltage readings for silicon diode below
VD=[                                    ];
% store current readings for silicon diode below
ID=[                                    ];
% store voltage readings for Zener diode below
VDz=[                                   ];
% store current readings for Zener diode below
IDz=[                                   ];
figure(1)
plot(VD,ID,'-dk',VDz,IDz,'-*k')
axis([-6 1 -10 12])
grid on
legend('silicon diode','Zener diode')
title('Graph 1 :The i-v characteristics for a silicon diode and a Zener diode')
xlabel('VD (V)')
ylabel('ID (mA)')
figure (2)
plot(VD,ID,'-dk')
axis([0 1 0 12])
grid on
title('Graph 2: The forward i-v characteristic of a silicon diode')
xlabel('VD (V)')
ylabel('ID (mA)')
```

```
% plotting ID-VDS characteristics for different values of VGS for NMOS
clf
VDS=[0 0.02 0.05 0.1 0.2 0.5 1 2];
% store current readings for VGS1 below
ID1=[                                   ];
% store current readings for VGS2 below
ID2=[                                   ];
% store current readings for VGS3 below
ID3=[                                   ];
figure(1)
plot(VDS,ID1,'-ob',VDS,ID2,'-dk',VDS,ID3,'-*r')
grid on
legend('VGS1','VGS2','VGS3')
title('The ID-VDS characteristics for NMOS')
xlabel('VDS (V)')
ylabel('ID (mA)')
```

Appendix B: Fundamentals of Electronics Lab Equipment List		
Lab	Equipment	Details
Lab 1	Power Supply	
	DMM	
	silicon diodes	1N4001 (2)
	LED	(1)
	Zener diode	4.3 V or 4.7 V
	Ge diode	
	Resistor	1 kΩ
	Rastered socket panel	
	Bridging plugs	
	wires	
Lab 2	Power Supply	
	DMM	
	silicon diode	1N4001
	Zener diode	4.3 V or 4.7 V
	Resistor	1 kΩ
	Rastered socket panel	
	Bridging plugs	
	wires	
Lab 3	Signal generator	
	Oscilloscope	
	DMM	
	silicon diodes	1N4001 (2)
	Zener diodes	4.3 V or 4.7 V (2)
	Resistor	1 kΩ
	Rastered socket panel	
	Bridging plugs	
	wires	
Lab 4	Center-tapped xformer	
	Oscilloscope	
	DMM	
	silicon diodes	1N4001 (2)
	Capacitor	10 µF, 470 µF
	Zener diode	4.3 V or 4.7 V
	Resistance decade box	
	Resistor	100 Ω
	Rastered socket panel	
	Bridging plugs	
	wires	
Lab 5	OrCAD Software	Demo version of OrCAD (Capture & PSpice)
Lab 6	Dual Power Supply	
	Signal generator	
	Oscilloscope	
	DMM	
	741 op amp	
	LEDs	(2)
	LDR	
	Resistors	1 kΩ, 10 kΩ, 100 kΩ, 27 kΩ, 39 kΩ
	Rastered socket panel	
	Bridging plugs	
	wires	

Lab 7	Power Supply	
	DMM	(2)
	NMOSFET	IRF620
	Resistor	1 kΩ
	Rastered socket panel	
	Bridging plugs	
	wires	
Lab 8	Power Supply	
	Signal generator	
	Oscilloscope	
	NMOSFET	IRF620
	Resistor	1 kΩ, 10 kΩ
	Capacitors	10 nF, 100 nF
	Rastered socket panel	
	Bridging plugs	
	wires	
Lab 9	Power Supply	
	DMM	
	BJT	BD137
	Resistors	1 kΩ, 68 kΩ
	Rastered socket panel	
	Bridging plugs	
	wires	
Lab 10	Power Supply	
	Signal generator	
	Oscilloscope	
	DMM	
	BJT	BD137
	Resistors	470 Ω, 4.7 kΩ, 47 kΩ, 5.6 kΩ
	Capacitors	2.2 µF (2), 470 µF
	Rastered socket panel	
	Bridging plugs	
	wires	

Appendix C

FAIRCHILD

November 2014

1N4001 - 1N4007
General-Purpose Rectifiers

Features

- Low Forward Voltage Drop
- High Surge Current Capability

DO-41

COLOR BAND DENOTES CATHODE

Ordering Information

Part Number	Top Mark	Package	Packing Method
1N4001	1N4001	DO-204AL (DO-41)	Tape and Reel
1N4002	1N4002	DO-204AL (DO-41)	Tape and Reel
1N4003	1N4003	DO-204AL (DO-41)	Tape and Reel
1N4004	1N4004	DO-204AL (DO-41)	Tape and Reel
1N4005	1N4005	DO-204AL (DO-41)	Tape and Reel
1N4006	1N4006	DO-204AL (DO-41)	Tape and Reel
1N4007	1N4007	DO-204AL (DO-41)	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value							Unit
		1N 4001	1N 4002	1N 4003	1N 4004	1N 4005	1N 4006	1N 4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current .375 " Lead Length at T_A = 75°C	1.0							A
I_{FSM}	Non-Repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
I^2t	Rating for Fusing (t < 8.3 ms)	3.7							A^2sec
T_{STG}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

Thermal Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	°C/W

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Value	Unit
V_F	Forward Voltage	I_F = 1.0 A	1.1	V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle	T_A = 75°C	30	µA
I_R	Reverse Current at Rated V_R	T_A = 25°C	5.0	µA
		T_A = 100°C	50	
C_T	Total Capacitance	V_R = 4.0 V, f = 1.0 MHz	15	pF

Typical Performance Characteristics

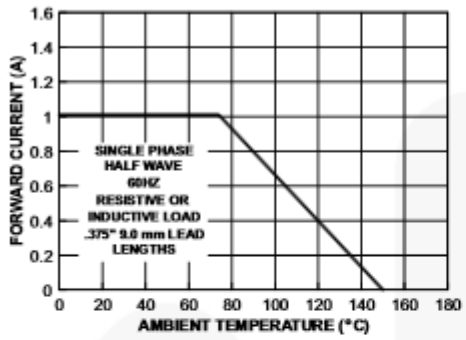


Figure 1. Forward Current Derating Curve

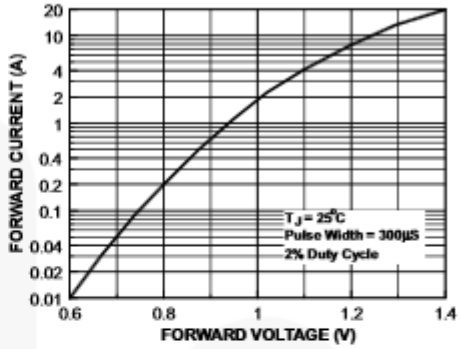


Figure 2. Forward Characteristics

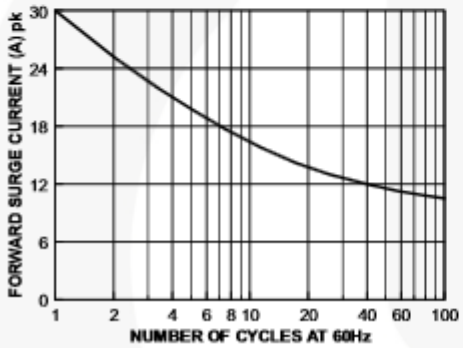


Figure 3. Non-Repetitive Surge Current

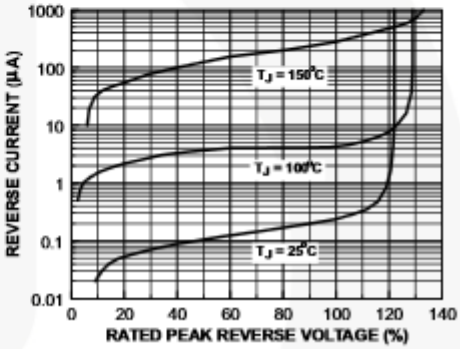


Figure 4. Reverse Characteristics

Appendix D

ZENER DIODE TABLE								
Volt	0.4 Watt		0.5 Watt		1 Watt		5 Watt	
2.4			1N5221	1N4617		UZ87=UZ88		UZ51=52=53
2.5			1N5222			UZ81=UZ82		UZ57=58=59
2.7			1N5223	1N4618				
2.8			1N5224					
3.0			1N5225	1N4619				
3.3	1N746		1N5226	1N4620	1N4728		1N5333	
3.6	1N747		1N5227	1N4621	1N4729		1N5334	
3.9	1N748		1N5228	1N4622	1N4730		1N5335	
4.3	1N749		1N5229	1N4623	1N4731		1N5336	
4.7	1N750		1N5230	1N4624	1N4732		1N5337	
5.1	1N751		1N5231	1N4625	1N4733		1N5338	
5.6	1N752		1N5232	1N4626	1N4734		1N5339	
6.0			1N5233	1N469			1N5340	
6.2	1N753		1N5234	1N4627	1N4735		1N5341	
6.8	1N754	1N957	1N5235	1N4628	1N4736	UZ8806	1N5342	UZ5806
7.5	1N755	1N958	1N5236	1N4629	1N4737	UZ8807	1N5343	UZ5807
8.2	1N756	1N959	1N5237	1N4630	1N4738	UZ8808	1N5344	UZ5808
8.7			1N5238	1N4695			1N5345	
9.1	1N757	1N960	1N5239	1N4631	1N4739	UZ8809	1N5346	UZ5809
10.0	1N758	1N961	1N5240	1N4632	1N4740	UZ8810	1N5347	UZ5810
11.0		1N962	1N5241	1N4633	1N4741		1N5348	
12.0	1N759	1N963	1N5242	1N4634	1N4742	UZ8812	1N5349	UZ5812
13.0	1N717	1N964	1N5243	1N4635	1N4743	UZ8813	1N5350	UZ5813
14.0			1N5244				1N5351	UZ5814
15.0	1N718	1N965	1N5245	1N4636	1N4744	UZ8815	1N5352	UZ5815
16.0	1N719	1N966	1N5246	1N4637	1N4745	UZ8816	1N5353	UZ5816
17.0			1N5247				1N5354	
18.0	1N720	1N967	1N5248	1N4638	1N4746	UZ8818	1N5355	UZ5818
19.0			1N5249				1N5356	
20.0	1N721	1N968	1N5250	1N4639	1N4747	UZ8820	1N5357	UZ5820
22.0	1N722	1N969	1N5251	1N4640	1N4748	UZ8822	1N5358	UZ5822
24.0	1N723	1N970	1N5252	1N4641	1N4749	UZ8824	1N5359	UZ5824
25.0			1N5253				1N5360	
27.0	1N724	1N971	1N5254	1N4642	1N4750	UZ8827	1N5361	UZ5827
28.0			1N5255				1N5362	
30.0	1N725	1N972	1N5256	1N4643	1N4751	UZ8830	1N5363	UZ5830
33.0	1N726	1N973	1N5257	1N4644	1N4752	UZ8833	1N5364	UZ5833
36.0	1N727	1N974	1N5258	1N4645	1N4753	UZ8836	1N5365	UZ5836
39.0	1N728	1N975	1N5259	1N4646	1N4754	UZ8840	1N5366	UZ5840
43.0	1N729	1N976	1N5260	1N4647	1N4755		1N5367	
47.0	1N730	1N977	1N5261	1N4648	1N4756	UZ8845	1N5368	
51.0	1N731	1N978	1N5262		1N4757	UZ8850	1N5369	UZ5850
56.0	1N732	1N979	1N5263		1N4758	UZ8856	1N5370	UZ5856
60.0			1N5264				1N5371	UZ5860
62.0	1N733	1N980	1N5265		1N4759	UZ8860	1N5372	
68.0	1N734	1N981	1N5266		1N4760	UZ8870	1N5373	
75.0	1N735	1N982	1N5267		1N4761	UZ8875	1N5374	UZ5875
82.0	1N736	1N983	1N5268		1N4762	UZ8880	1N5375	UZ5880
87.0			1N5269				1N5376	
91.0	1N737	1N984	1N5270		1N4763	UZ8890	1N5377	UZ5890
100.0	1N738	1N985	1N5271		1N4764	UZ8110	1N5378	UZ5310
110.0	1N739	1N986	1N5272			UZ8111	1N5379	UZ5311
120.0	1N740	1N987	1N5273			UZ8112	1N5380	UZ5312
130.0	1N741	1N988	1N5274			UZ8113	1N5381	UZ5313
140.0			1N5275			UZ8114	1N5382	UZ5314
150.0	1N742	1N989	1N5276			UZ8115	1N5383	UZ5315
160.0	1N743	1N990	1N5277			UZ8116	1N5384	UZ5316
170.0			1N5278			UZ8117	1N5385	UZ5317
180.0	1N744	1N991	1N5279			UZ8118	1N5386	UZ5318
190.0			1N5280			UZ8119	1N5387	UZ5319
200.0	1N745	1N992	1N5281			UZ8120	1N5388	UZ5320

Appendix E

Standard Components Values

Standard Resistor Values (±5%)						
1.0	10	100	1.0K	10K	100K	1.0M
1.1	11	110	1.1K	11K	110K	1.1M
1.2	12	120	1.2K	12K	120K	1.2M
1.3	13	130	1.3K	13K	130K	1.3M
1.5	15	150	1.5K	15K	150K	1.5M
1.6	16	160	1.6K	16K	160K	1.6M
1.8	18	180	1.8K	18K	180K	1.8M
2.0	20	200	2.0K	20K	200K	2.0M
2.2	22	220	2.2K	22K	220K	2.2M
2.4	24	240	2.4K	24K	240K	2.4M
2.7	27	270	2.7K	27K	270K	2.7M
3.0	30	300	3.0K	30K	300K	3.0M
3.3	33	330	3.3K	33K	330K	3.3M
3.6	36	360	3.6K	36K	360K	3.6M
3.9	39	390	3.9K	39K	390K	3.9M
4.3	43	430	4.3K	43K	430K	4.3M
4.7	47	470	4.7K	47K	470K	4.7M
5.1	51	510	5.1K	51K	510K	5.1M
5.6	56	560	5.6K	56K	560K	5.6M
6.2	62	620	6.2K	62K	620K	6.2M
6.8	68	680	6.8K	68K	680K	6.8M
7.5	75	750	7.5K	75K	750K	7.5M
8.2	82	820	8.2K	82K	820K	8.2M
9.1	91	910	9.1K	91K	910K	9.1M

Standard Capacitor Values (±10%)						
10pF	100pF	1000pF	.010µF	.10µF	1.0µF	10µF
12pF	120pF	1200pF	.012µF	.12µF	1.2µF	
15pF	150pF	1500pF	.015µF	.15µF	1.5µF	
18pF	180pF	1800pF	.018µF	.18µF	1.8µF	
22pF	220pF	2200pF	.022µF	.22µF	2.2µF	22µF
27pF	270pF	2700pF	.027µF	.27µF	2.7µF	
33pF	330pF	3300pF	.033µF	.33µF	3.3µF	33µF
39pF	390pF	3900pF	.039µF	.39µF	3.9µF	
47pF	470pF	4700pF	.047µF	.47µF	4.7µF	47uF
56pF	560pF	5600pF	.056µF	.56µF	5.6µF	
68pF	680pF	6800pF	.068µF	.68µF	6.8µF	
82pF	820pF	8200pF	.082µF	.82µF	8.2µF	