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| ksuBlackLogo.jpg | Computer Engineering Dept.  College of Computer and Information Sciences  King Saud University | CEN 317: Logic Design Laboratory-II  Prepared by: Eng. AbdulMAlik Rahhal |

**Experiment 4: Clock Divider and Timers**

**Objectives**

The purpose of this Exercise is to design and implement a Clock Divider so that it outputs 1Hz when its input clock is 50 MHz. This output is then used in the design of a real-time Clock. The designed circuit will be implemented on the Altera DE1 board.

**Preparation**

• Review counter and the 7-segment displays.

**Equipment Needed**

• ActiveHDL, Quartus II, and Altera DE1 Board.

**References**

•Altera DE1 Board user manual, and Exercises.

**Background**

Digital systems usually has a primary clock generating circuit which in most cases is derived from a crystal oscillator. But not all parts of digital systems needs the same clock some needs a higher clock rate some need a lower one. To get a lower clock rate from a higher one a clock divider is used.

For example, to get 1Hz clock rate from Altera DE1 board’s main clock which is a 50 MHz. The output of the *clock divider* is low for the first half of 50MHz, and then goes high for the second half. In other words, it is low for 25000000 clock periods and high for the second 25000000 clock period, as shown in **Figure 1**.



**Figure 1**: 1Hz from 50 MHz

**For this exercise, do:**

**Part I**

Design the *clock divider* that generates the 1Hz from the 50 MHz.

**Part II**

Use your design in Part I to design and implement a circuit on the DE1 board that acts as an especial real-time clock. It should display the minutes (from 0 to 5) on HEX3-2 and the seconds (from 0 to 10) on HEX1-0. Use the switches SW7-0 to preset the minute part of the time displayed by the clock.

**Prelab Assignments**

The recommended preparation for this laboratory exercise includes:

1. Verilog code for Part I
2. Simulation of the Verilog code for Part I
3. Verilog code for Part II
4. Simulation of the Verilog code for Part I

**Lab Assignments**

For each Part, perform the following steps:

1. Create a new Quartus II project for your circuit.

2. Include your Verilog file for your design. Use switch SWs on the DE1 board as inputs, and LEDs for the outputs.

3. Include in your project the required pin assignments for the DE1 board.

4. Compile the project.

5. Download the compiled circuit into the FPGA chip. Test the functionality of your design by toggling the inputs and observing the outputs.

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