2nd Semester 1436/1437 (2015/2016)
Date of Exam: 24th May, 2016

Department of Electrical Engg.
College of Engineering
King Saud University

EE 212: Electric Circuits Analysis

Final Examination

Time allowed: 3 Hours

Instructors: Prof. Nazar H. Malik, Prof. Saad M. Alghuwainum. & Dr. Yasin Khan

Student Name: .....

Student No.: .....

Section No.: .....

Final Exam. Mark (40): …….
Term Work Mark (60): …….
Total (100): ……. **Grade:** …….

Course Learning Objectives:

CLO-A: An ability to apply knowledge of mathematics, science, and engineering [5]
[*CLO-A = 40% each question*]

CLO-C: Ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability [2] **[*CLO-C = 20% each question*]**

CLO-E: Ability to identify, formulate, and solve engineering problems [5] **[*CLO-E = 40% each*]**

Questions	Full Mark	Marks obtained
1	20	
2	20	
3	20	
4	20	
5	20	
Total	**100**	

Answer all questions

Question #1 (a)

Use nodal analysis to determine V_1 and power being supplied by the dependent current source in the circuit shown in **Fig. 1(a).**

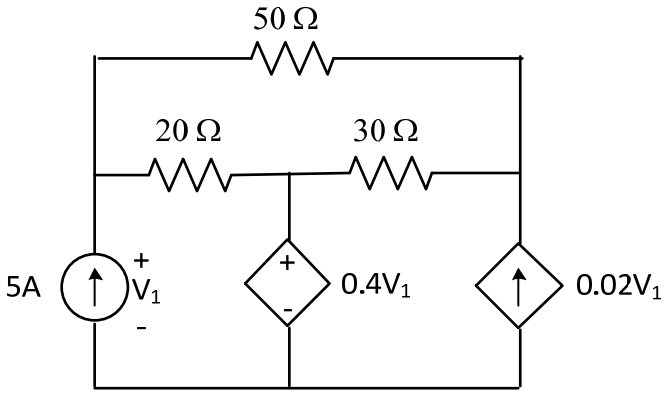

Fig.1(a)

Question #1 (b)

For the circuit shown in **Fig.1(b),** the switch *S* is closed for a long time. It is opened at *t=0.* Find i*(t) for* $t \geq 0$.

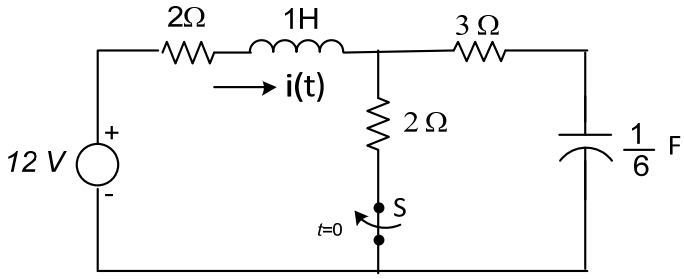

Fig.1(b)

Question #2 (a)

For the circuit shown in **Fig. 2 (a),** find V_o and I_o.

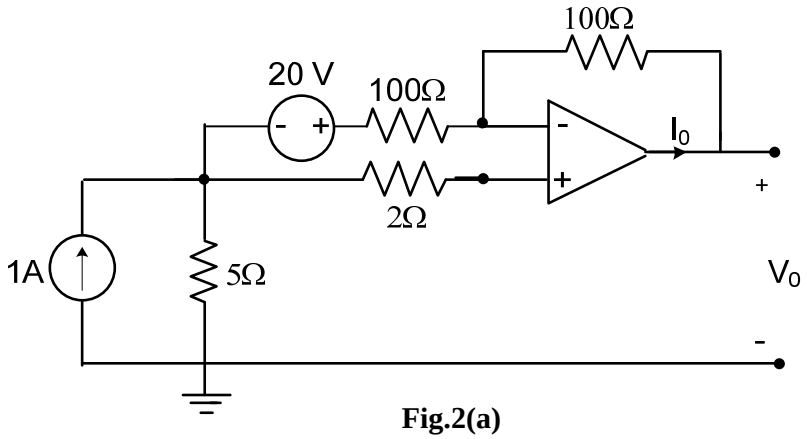

Fig.2(a)

Question #2 (b)

For the circuit shown in **Fig. 2 (b),** find V_o and I_o

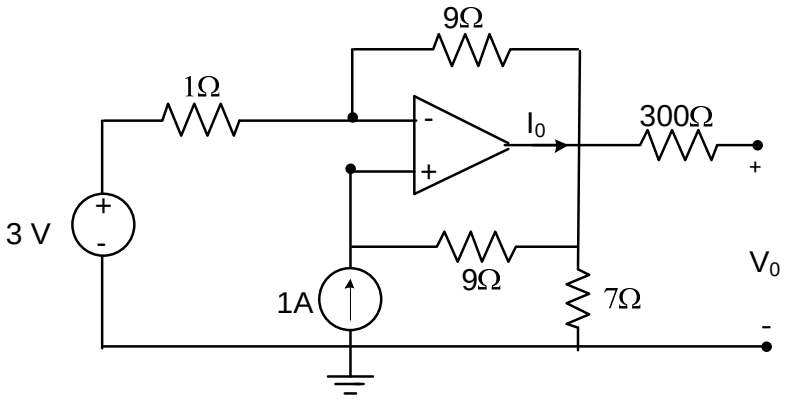

Fig.2(b)

Question #3 (a)

For the circuit shown in **Fig. 3(a),** the switch S has been opened for very long time. It is closed at time t=0. Find i*(t) for* $t \geq 0$ and sketch *i(t)* versus *t.*

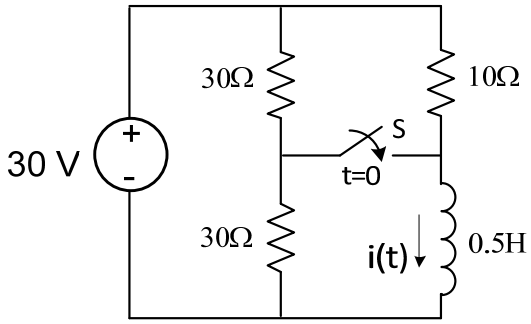

Fig.3(a)

Question #3(b)

For the circuit shown in **Fig. 3(b),** the switch S has been opened for very long time. It is closed at time t=0. Find *v(t) for* $t \geq 0$

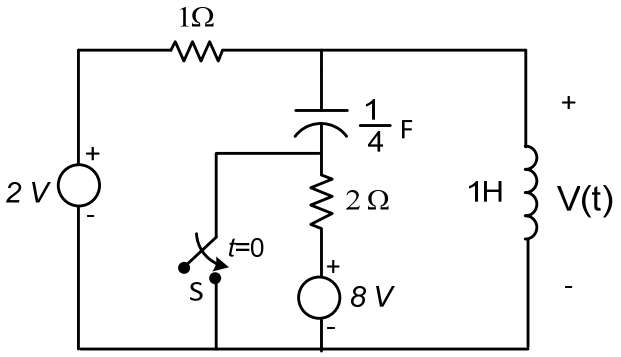

Fig.3(b)

Question #4 (a)

For the circuit shown in **Fig. 4(a),** calculate the following:

(i) $V_1(t)$ (ii) $V_2(t)$

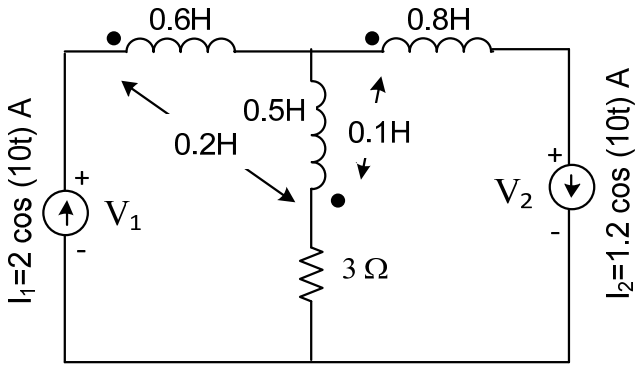

Fig.4(a)

Question #4(b)

(a) For the circuit shown in **Fig. 4(b),** the quality factor Q=3, calculate

(i) L (ii) ω_0 (iii) β

(iv) ω_1 and ω_2

(b) What type of filter is this, if output is taken:

(v) across R, (vi) across L, (vii) across C

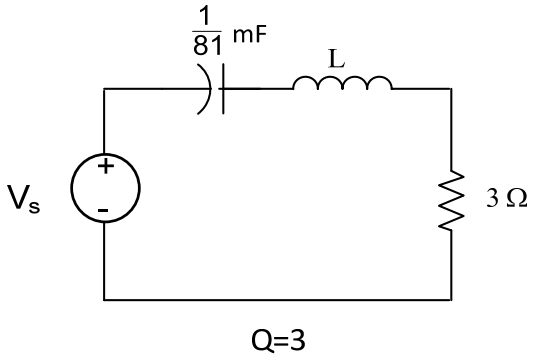

Fig.4(b)

Question #5(a)

For the circuit shown in **Fig. 5(a),** calculate the following:

(i) Transfer function H(s) $=\frac{I_0(s)}{I_s(s)}$

(ii) Poles and zeros of H(s)

(iii) What type of filter does this circuit represent?

(iv) If H(jω) is written as: $H(j\omega) = \frac{k}{(1+j\frac{\omega}{a})(1+j\frac{\omega}{b})}$ find *k*, *a* and *b*.

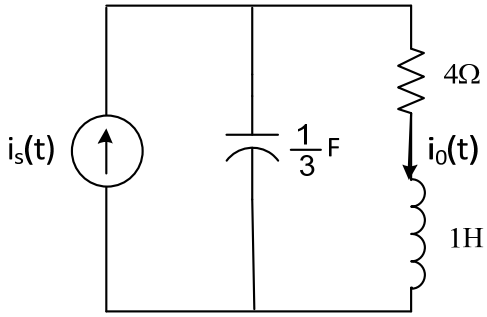

Fig.5(a)

Question #5(b)

(a) For the circuit shown in **Fig. 5(b),** use the given *Z*-parameters to determine V_2.

(b) Find an equivalent T-circuit for the two-port network which will have the given Z-parameters.

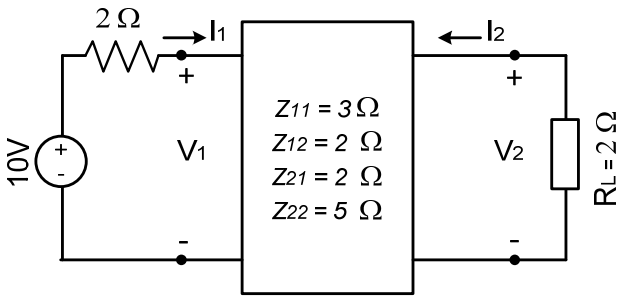

Fig.5(b)