	Q#1	Q#2	Total Marks

King Saud University
College of Engineering
Electrical Engineering Department
Student name: Student ID:

EE208: Logic Design
Mid Term Exam: Part#2
Time allowed: 60 Min
1st Semester 1426H-1427H

Question 1:

a) Use only one decoder 3/8 with complemented output to design a full adder circuit
(***hint***: the circuit has 3 input binary bits and two output functions sum & carry)

b) Write the function table of the ROM to implement the following function and compute its size

$$Y = \begin{cases} X + 15 & 0 \le X \le 5 \\ X^2 - 5 & 5 \le X \le 10 \\ X + 85 & 10 \le X \le 15 \end{cases} ;$$

Where X is a 4-bit unsigned binary number and Y is the ROM output code

Answer to question 1:

Question 2:

a) Design a 6X1 line Multiplexer using 4X1 line Multiplexers having separate enable inputs. Use block diagram construction.

b) A combinational logic circuit is defined by

$$F_1 (x,y,z) = \Sigma\, m(0,2,3,7) + \Sigma\, d(4,6)$$
$$F_2 (x,y,z) = \Sigma\, m(1,3) + \Sigma\, d(0,5,7)$$

Write the PLA program table using PLA having 3 inputs, 2 product terms, and 2 outputs

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Answer to question 2: