King Saud University
College of Engineering
Electrical Engineering Department

EE208: Logic Design
Mid Term Exam: Part#2
Time allowed: 60 Min

1st Semester 1425H

Question	Marks
First	
Second	
Total	

Question 1:

a) Use a MUX 4X1 to implement the logic function

$$F = ABC+B'C$$

Write the truth table and draw the circuit diagram

b) Compute the ROM size to implement the function

$$F = X^2 + 16$$

Where X is a 2 bit input number ; Write the truth table

Answer to question 1:

Answer to question 1:

Question 2:

a) Design a 4X16 decoder using 2X4 decoders having separate enable inputs. Use block diagram construction.

b) A combinational logic circuit is defined by

$F_1 = \Sigma (0,2,4,6)$
$F_2 = \Sigma (1,3,5)$

Implement the circuit using PLA having 3 inputs, 2 product terms, and 2 outputs
(**hin**t: Write the PLA program table only)

Answer to question 2:

Complete the answer to question 2: