Clock Generator 8284A

CEN433
King Saud University
Dr. Mohammed Amer Arafah

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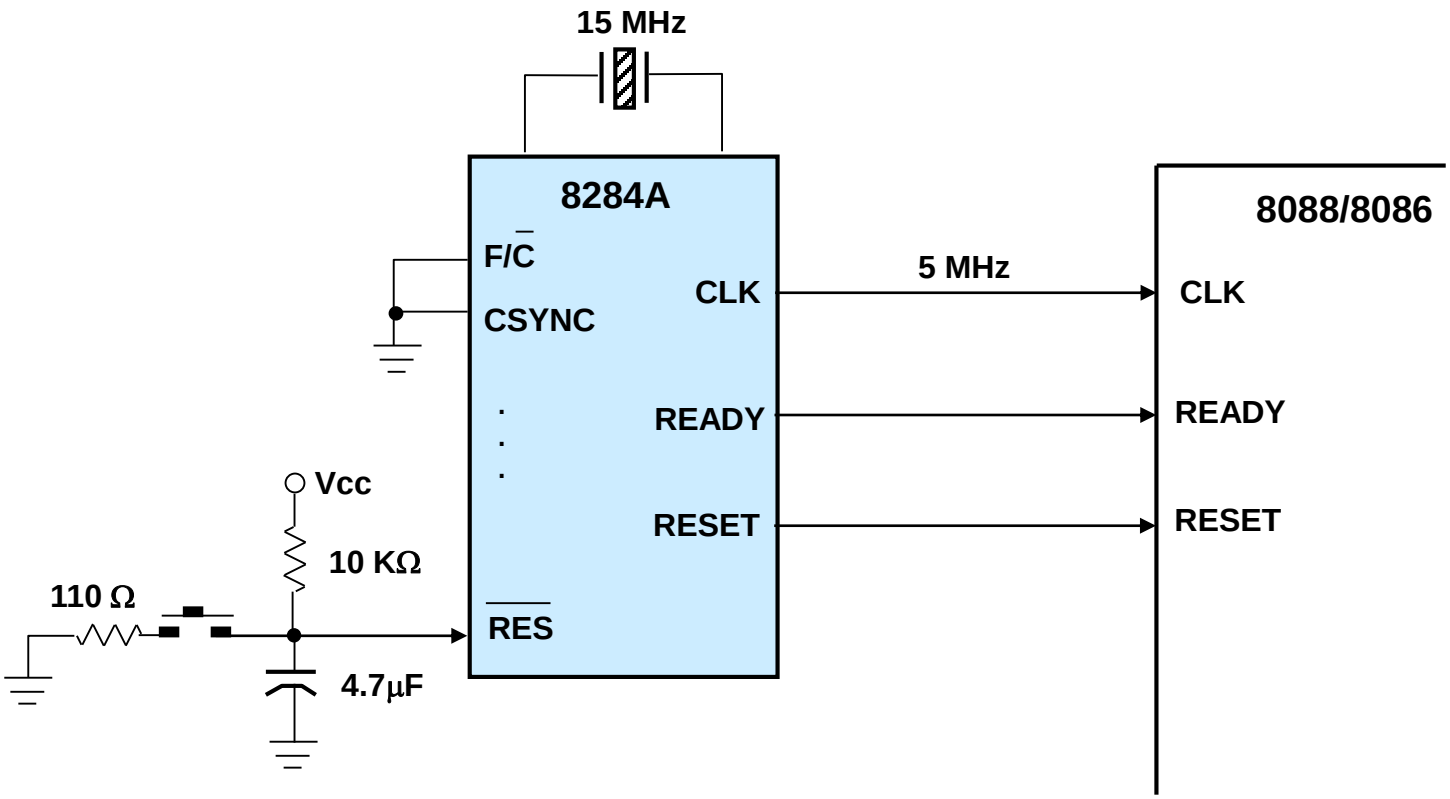

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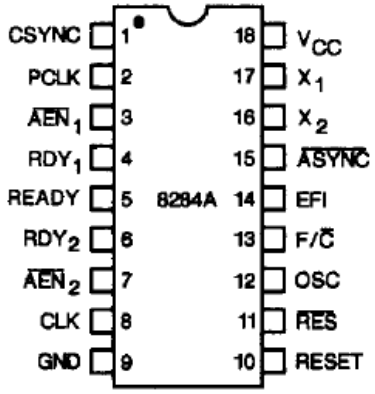

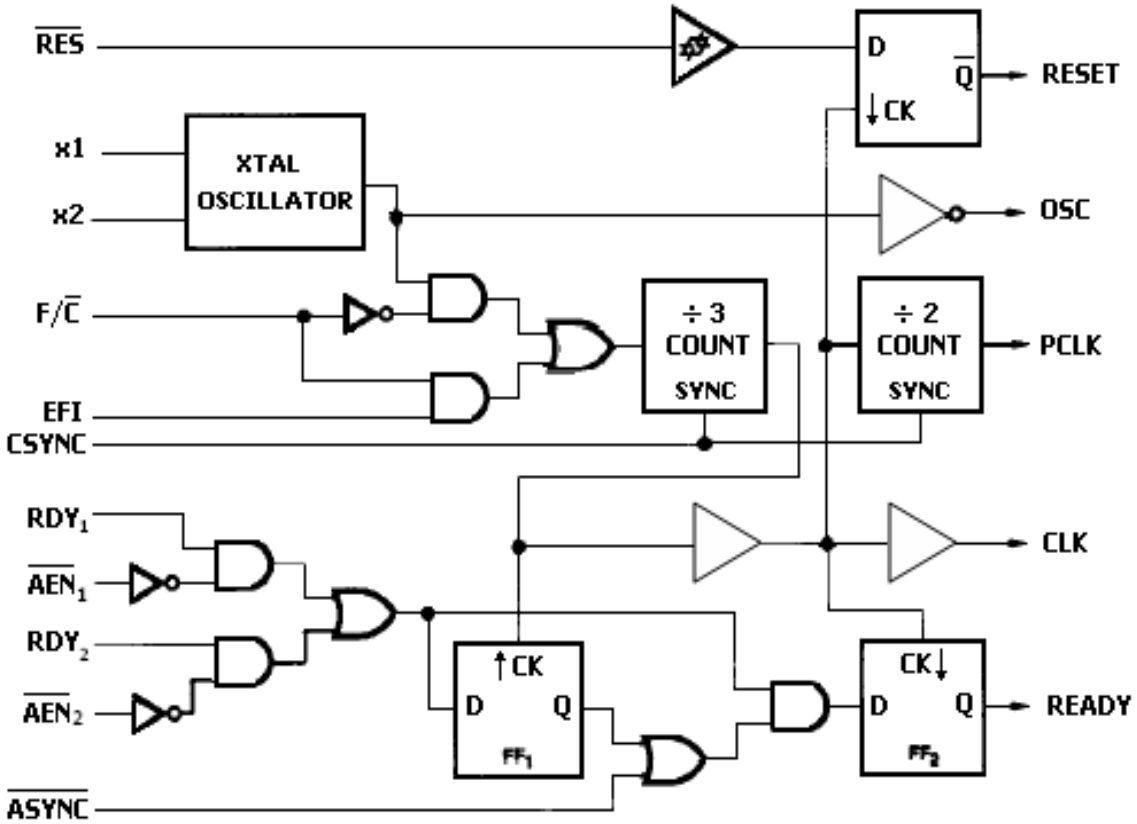

Pin Description

SYMBOL	NUMBER	TYPE	DESCRIPTION
$\overline{AEN1}$, $\overline{AEN2}$	3, 7	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non-Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY1, RDY2	4, 6	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	15	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH, a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	17, 16	I O	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency, (Note 1).
F/$\overline{C}$	13	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW. F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated for the EFI input, (Note 1).
EFI	14	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	12	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	11	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	10	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND	9		Ground
V_{CC}	18		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between V_{CC} and GND is recommended for decoupling.

NOTE:
1. If the crystal inputs are not used X1 must be tied to V_{CC} or GND and X2 should be left open.

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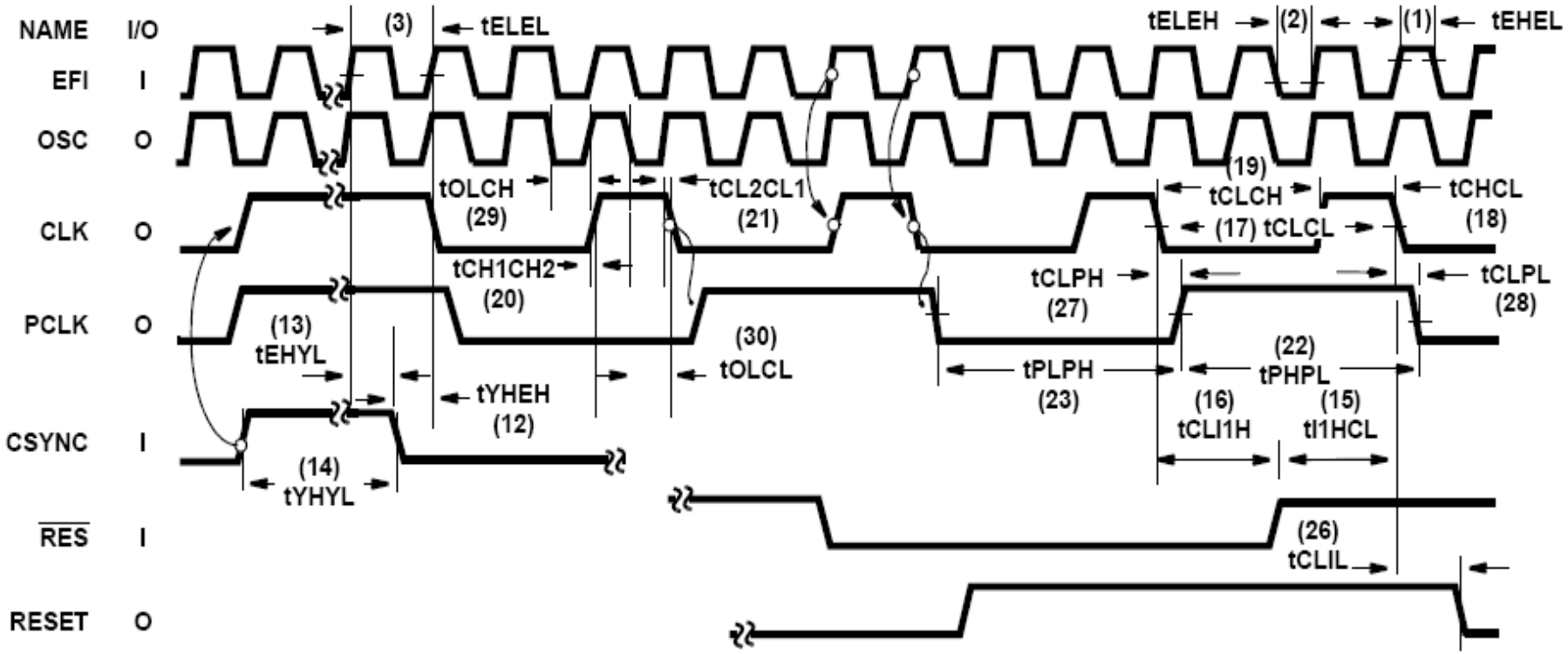

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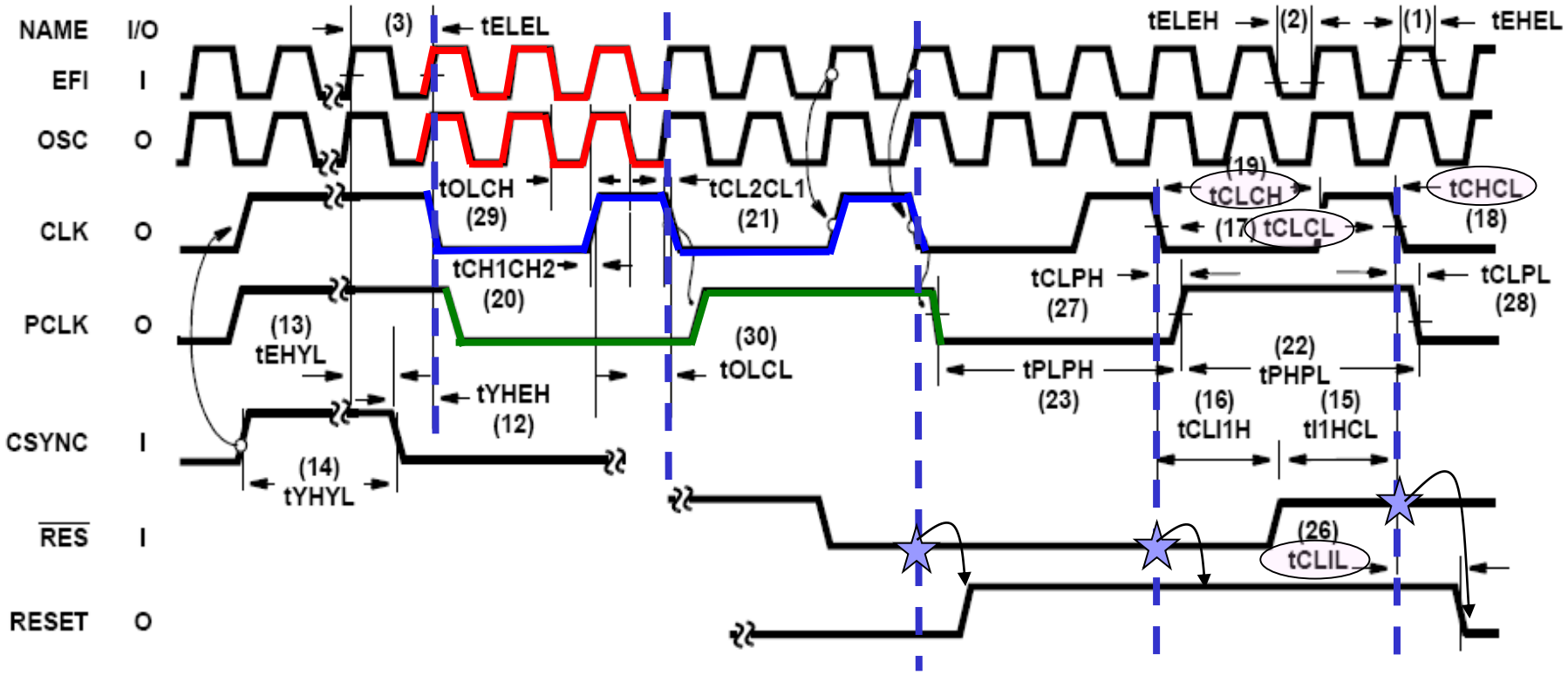
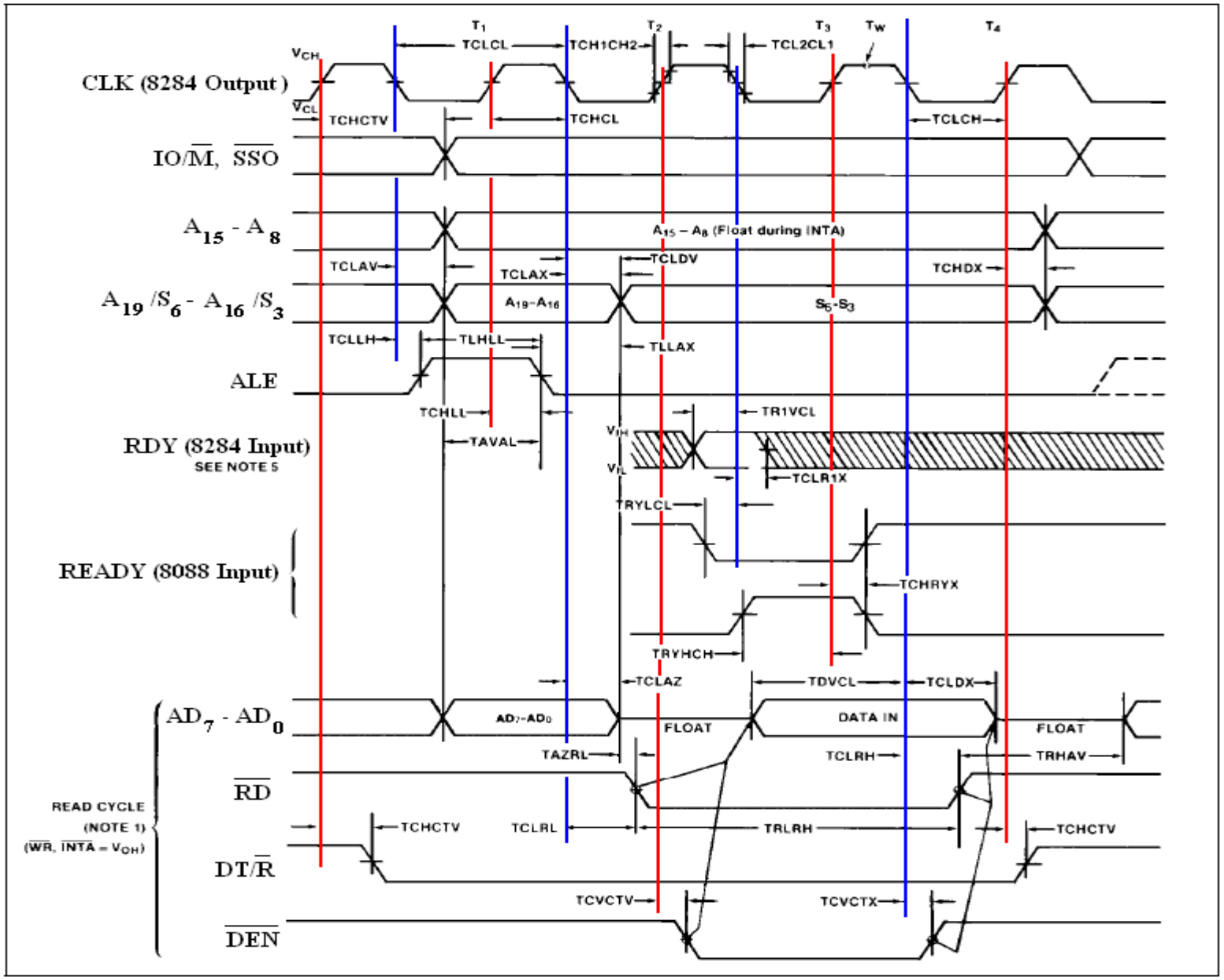
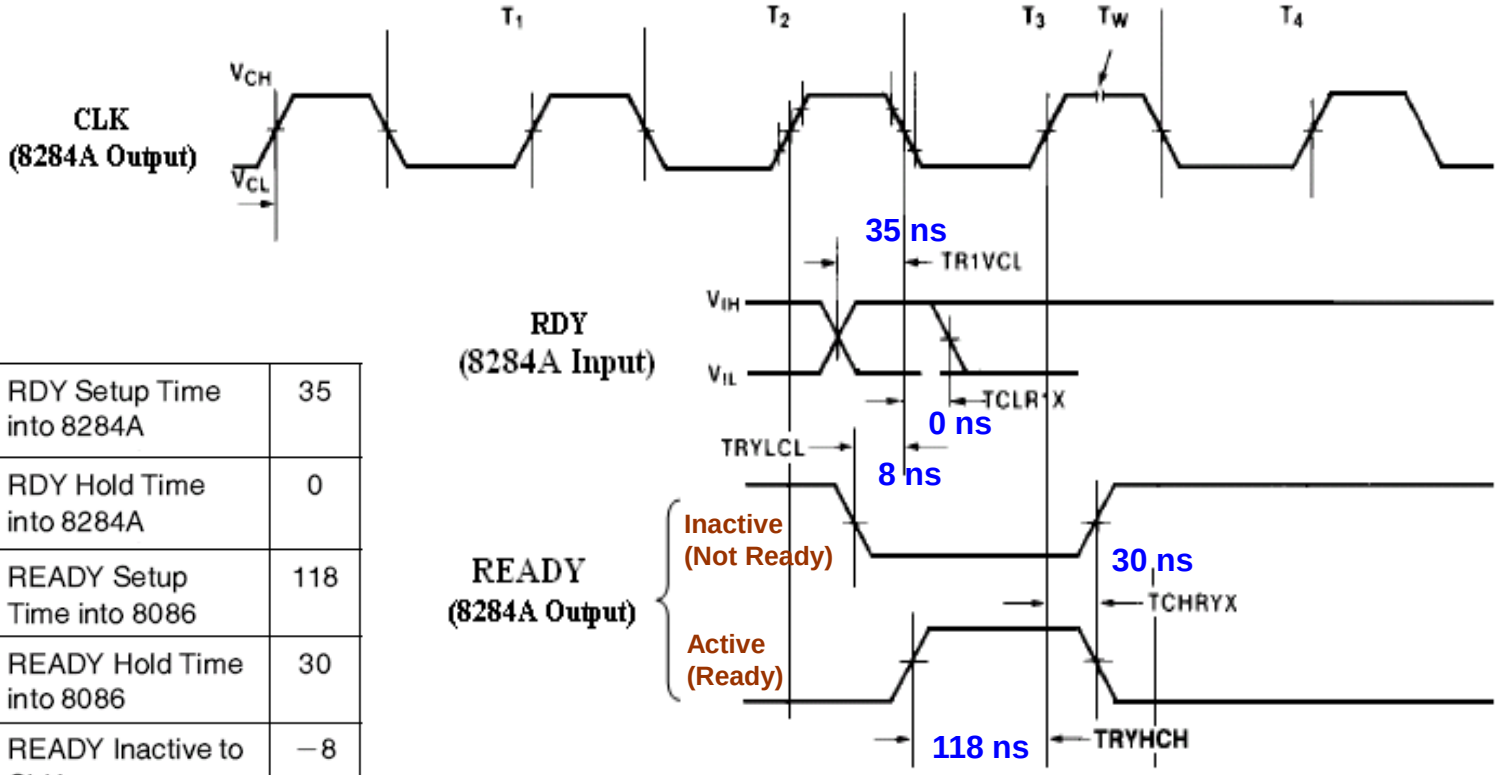


BUS TIMING—MINIMUM MODE SYSTEM

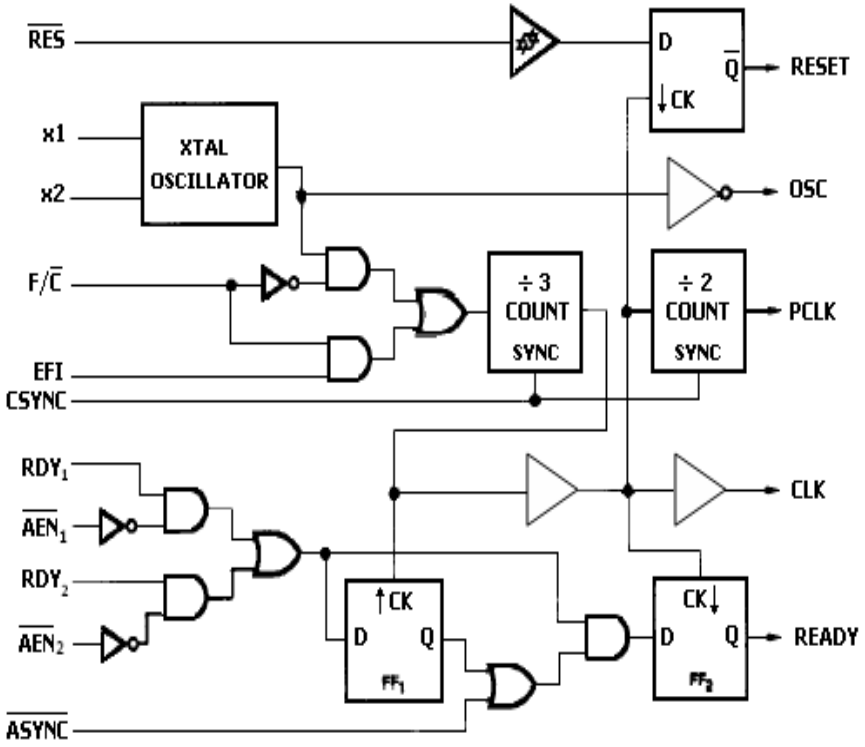


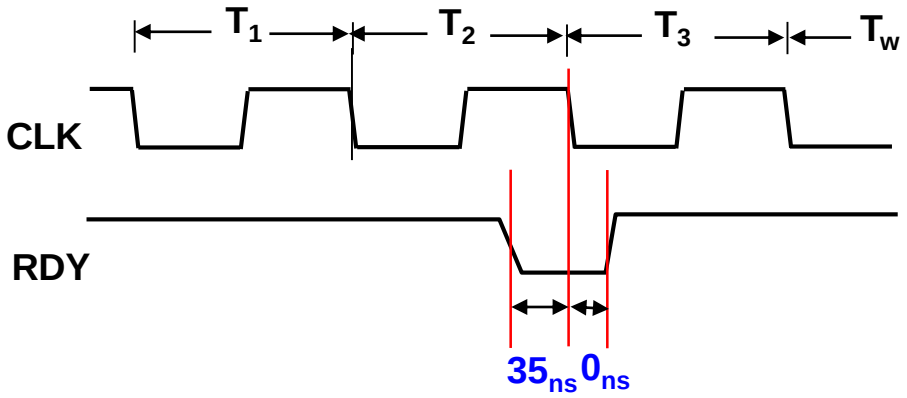
Ready and the Wait State

TR1VCL	RDY Setup Time into 8284A	35
TCLR1X	RDY Hold Time into 8284A	0
TRYHCH	READY Setup Time into 8086	118
TCHRYX	READY Hold Time into 8086	30
TRYLCL	READY Inactive to CLK	−8

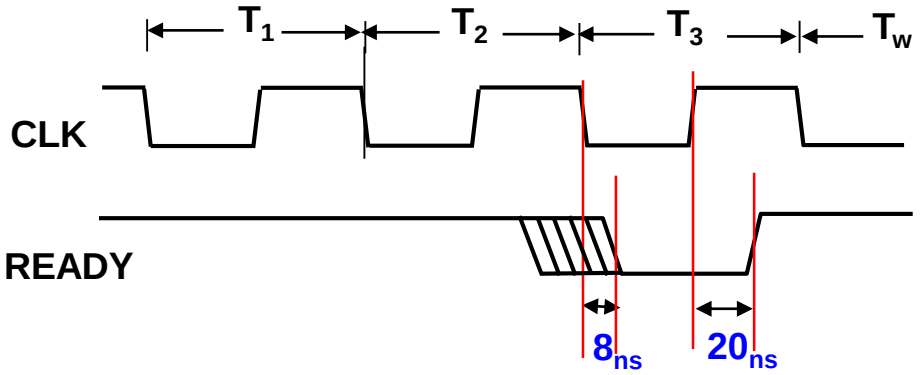


Ready and the Wait State



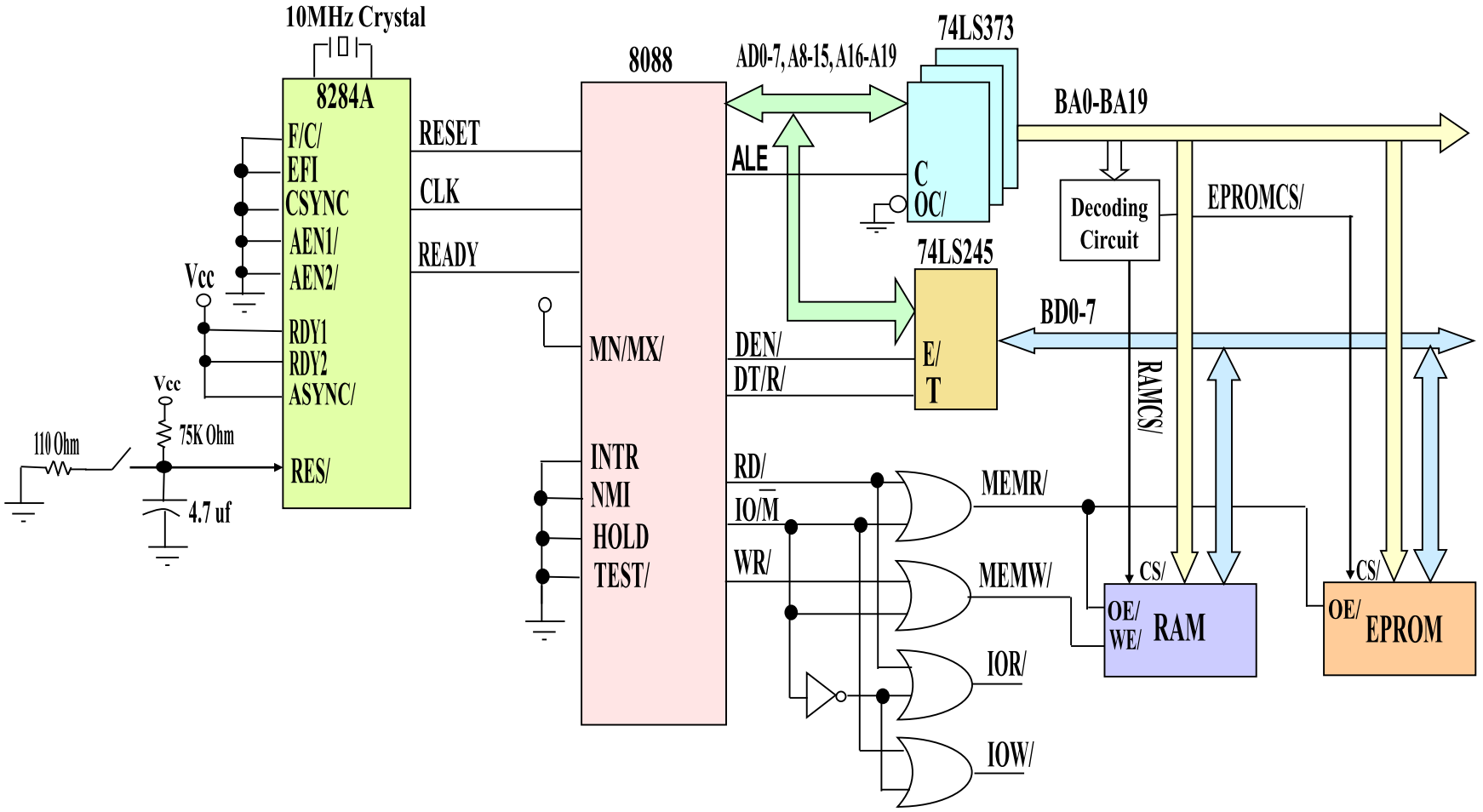


8284A RDY Input Timing Requirements

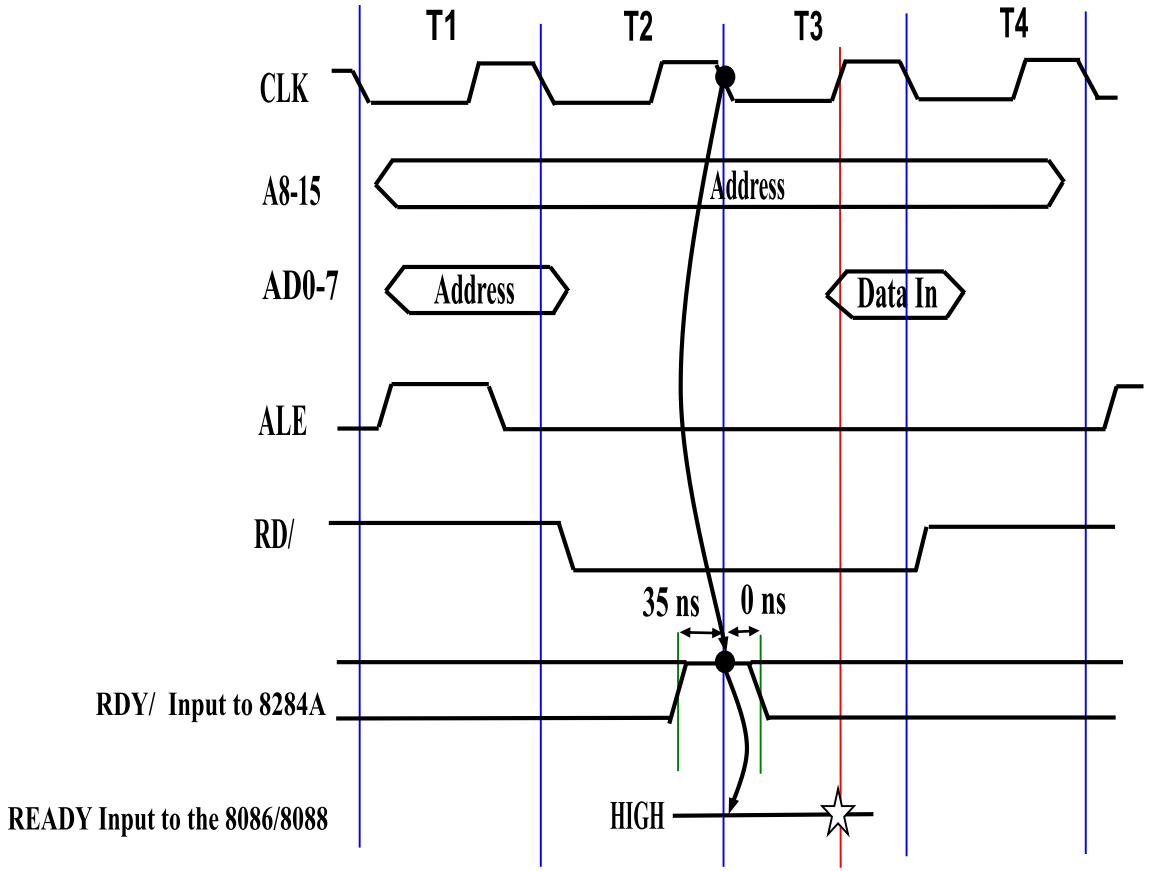


8088-2 READY Input Timing Requirements

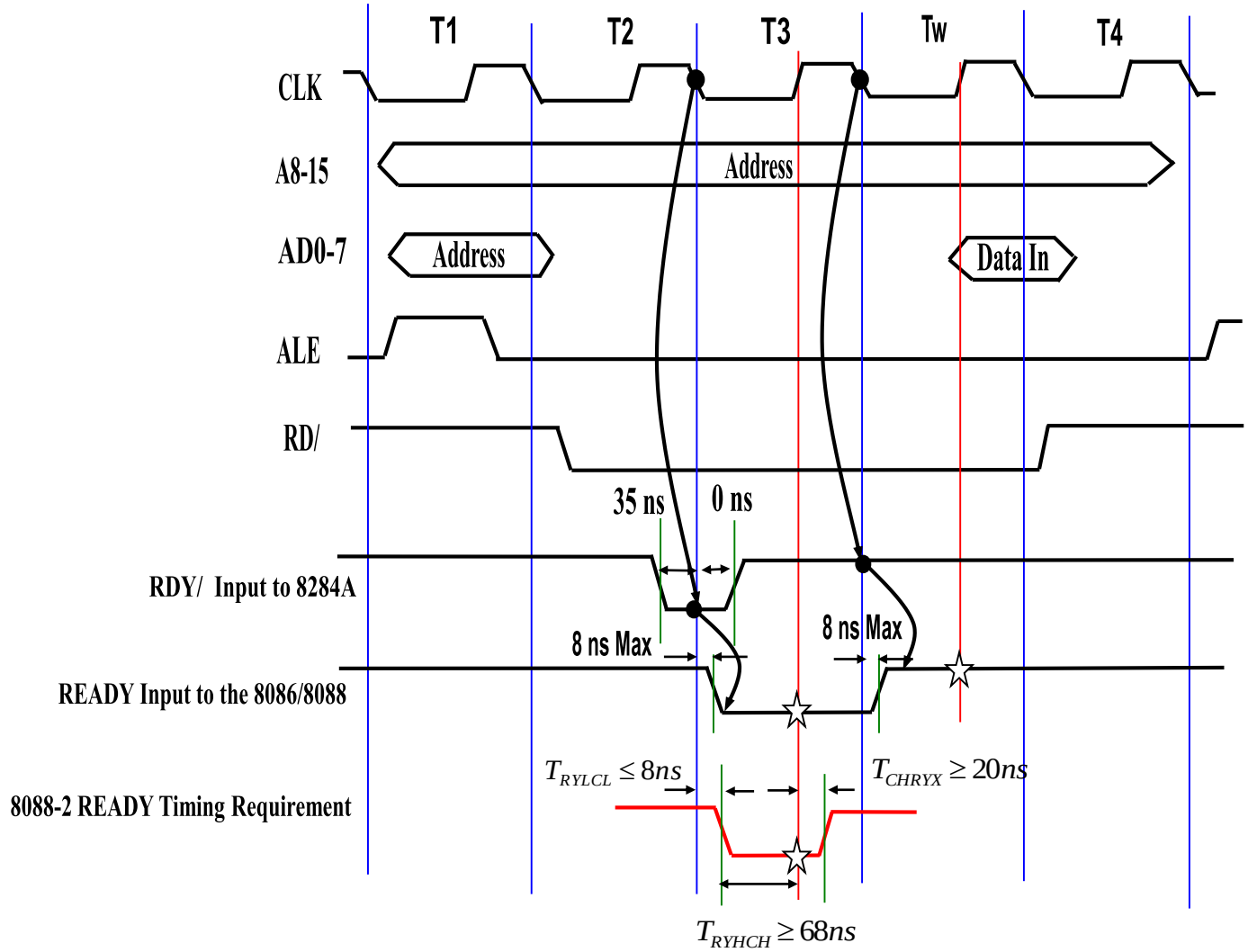
Minimum Mode 8088 System (Zero Wait State)



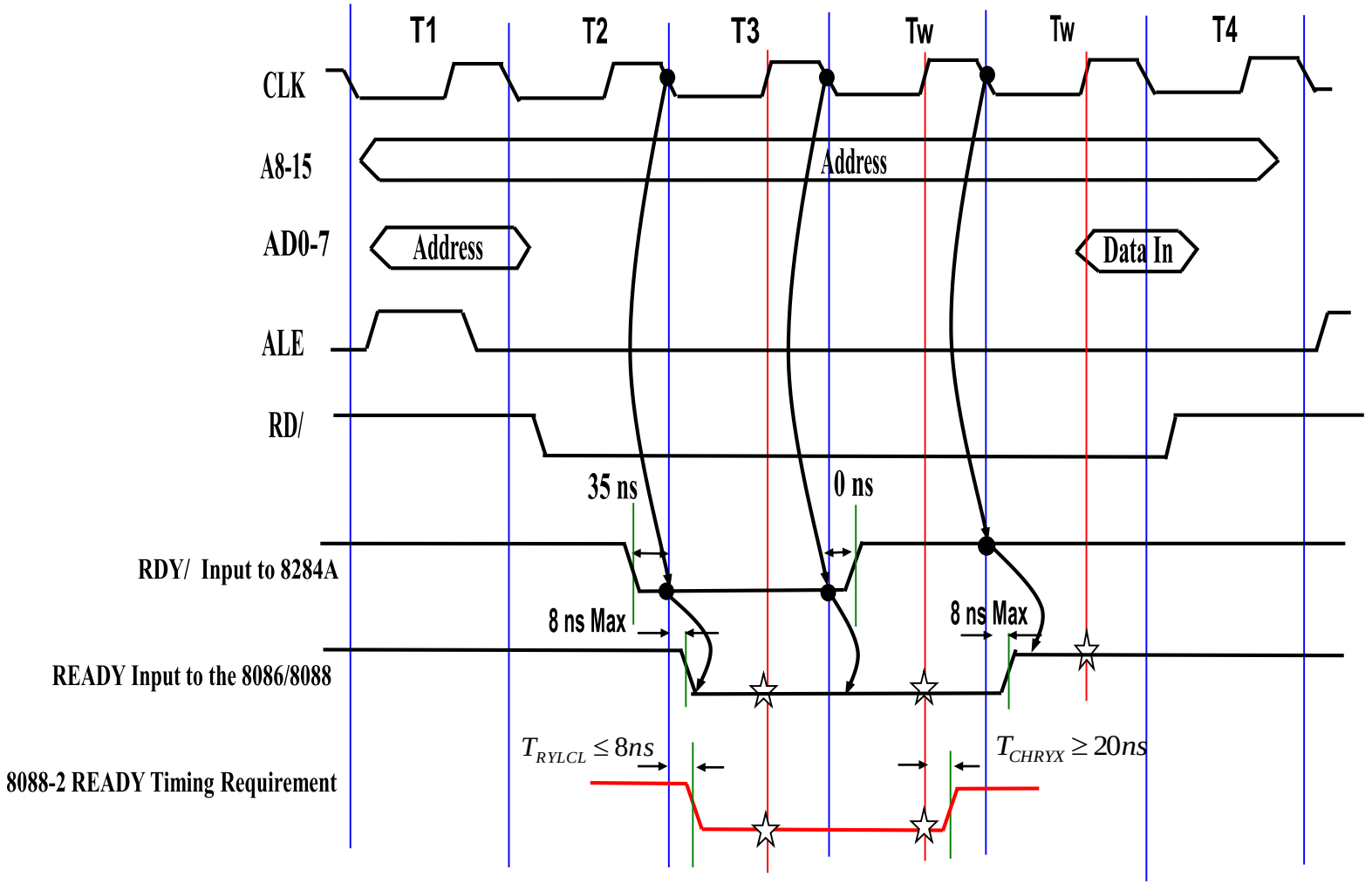
Zero Wait State



One Wait State



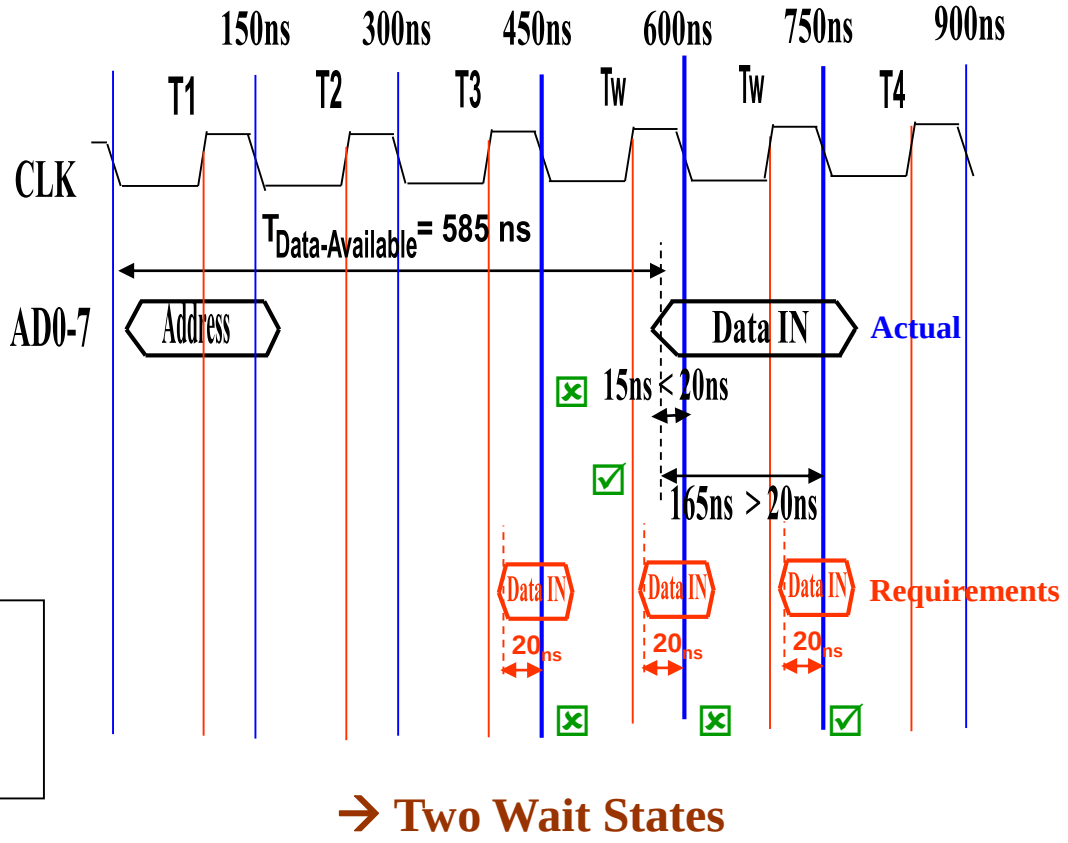
Two Wait States



Example

Assumptions:

- **A 20 MHz Crystal is used.**
- **CLK signal is used.**
- **$T_{Data\_Available}$= 585 ns.**

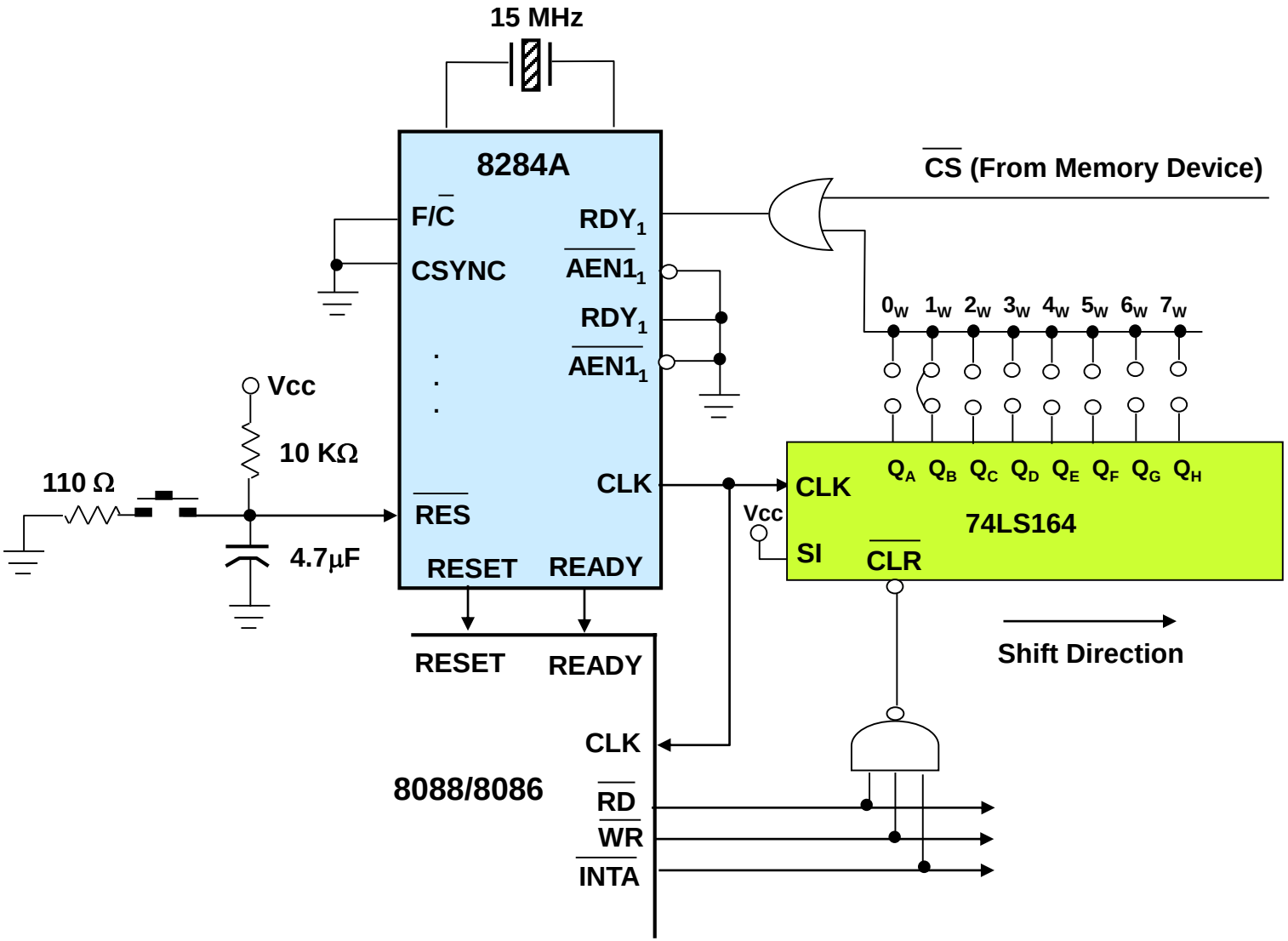


$$N = \left\lceil \frac{Tdata\_Available - 3T + 20)}{T} \right\rceil$$

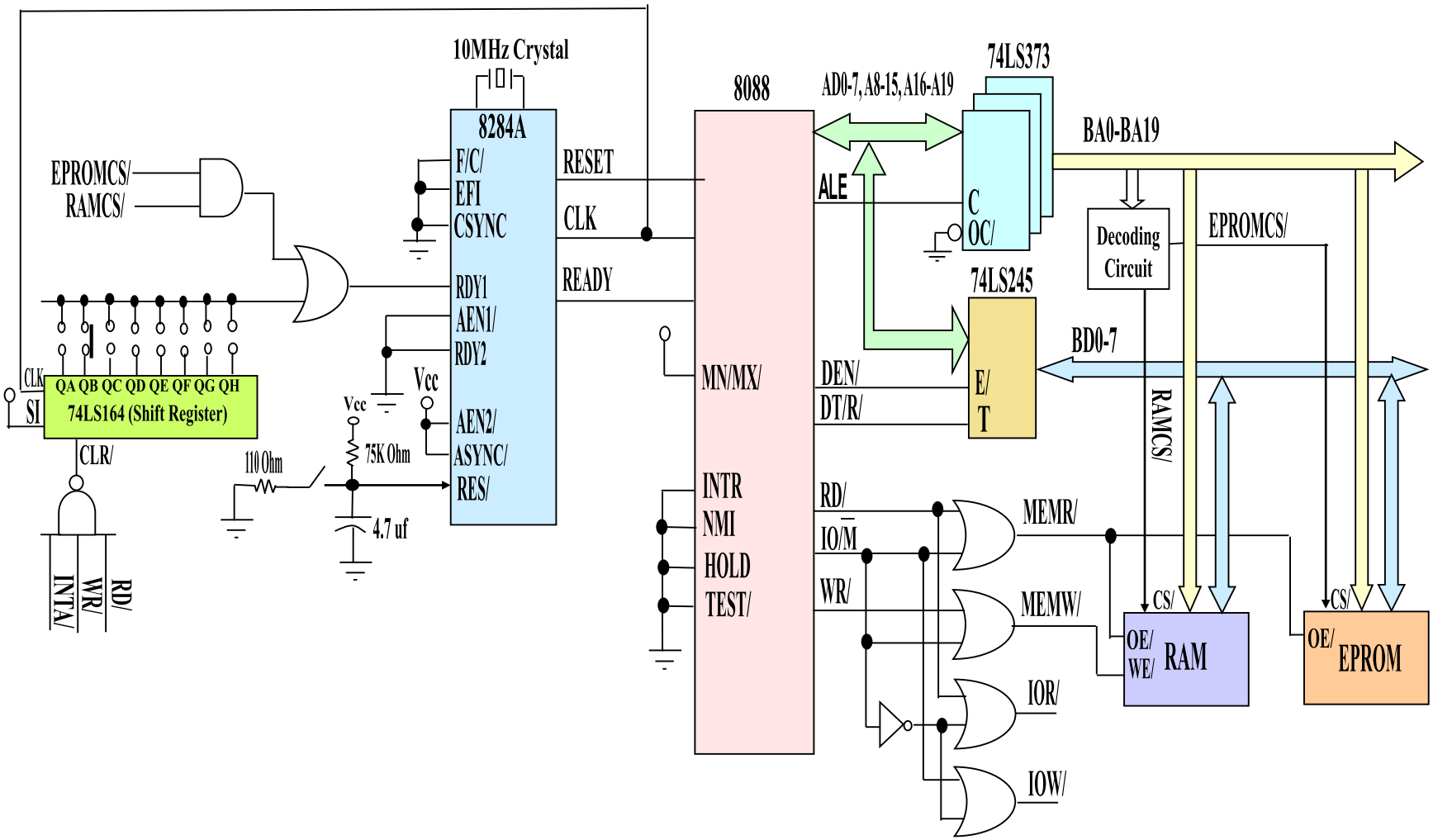
N = Ceiling[($T_{data\text{-}Available}$ - 3T + 20)/T]
→ N = Ceiling[(585-450+20)/150]
→ N = Ceiling[155/150]
→ N = 2

→ Two Wait States

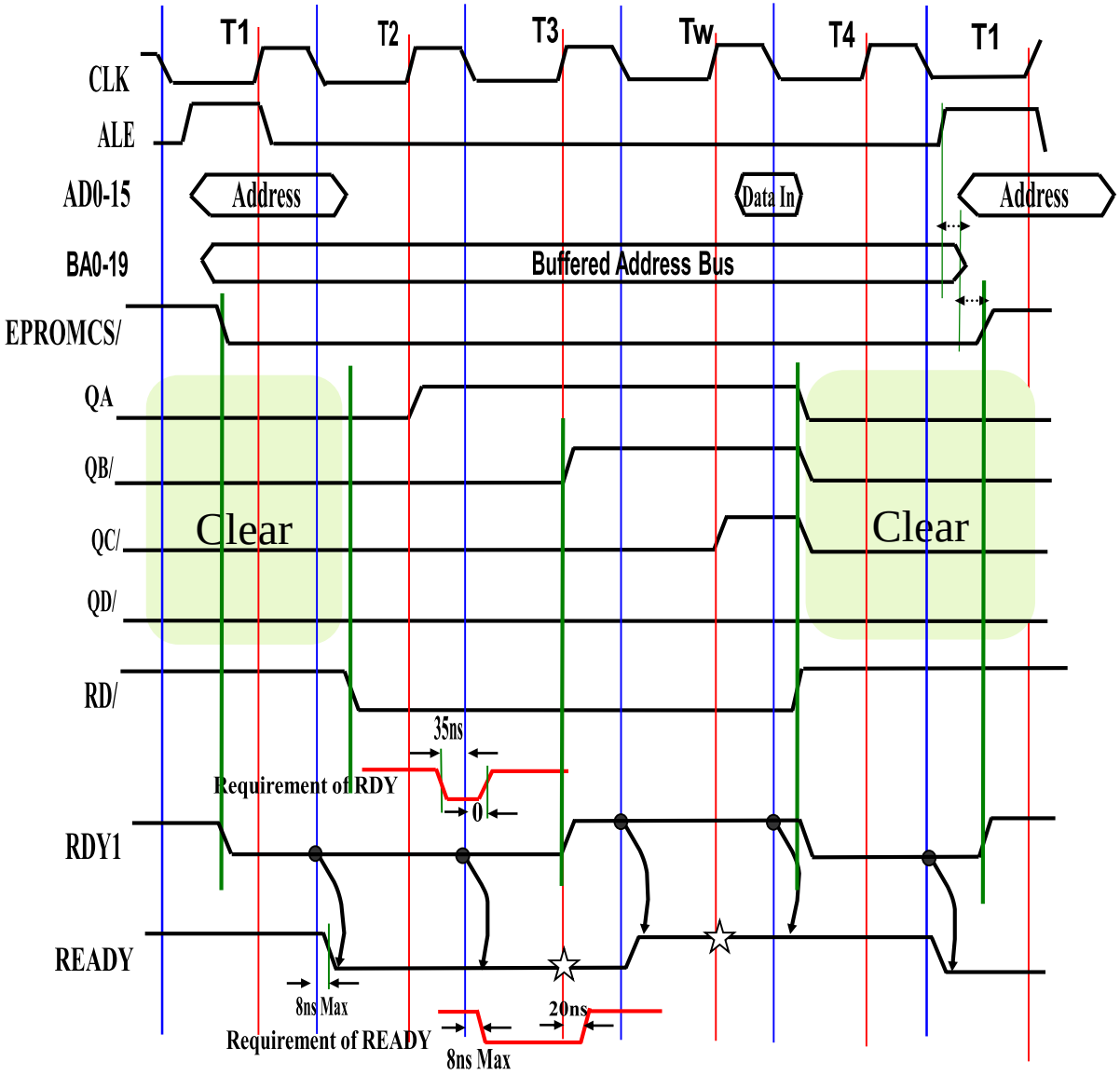
Wait State Generator Circuit



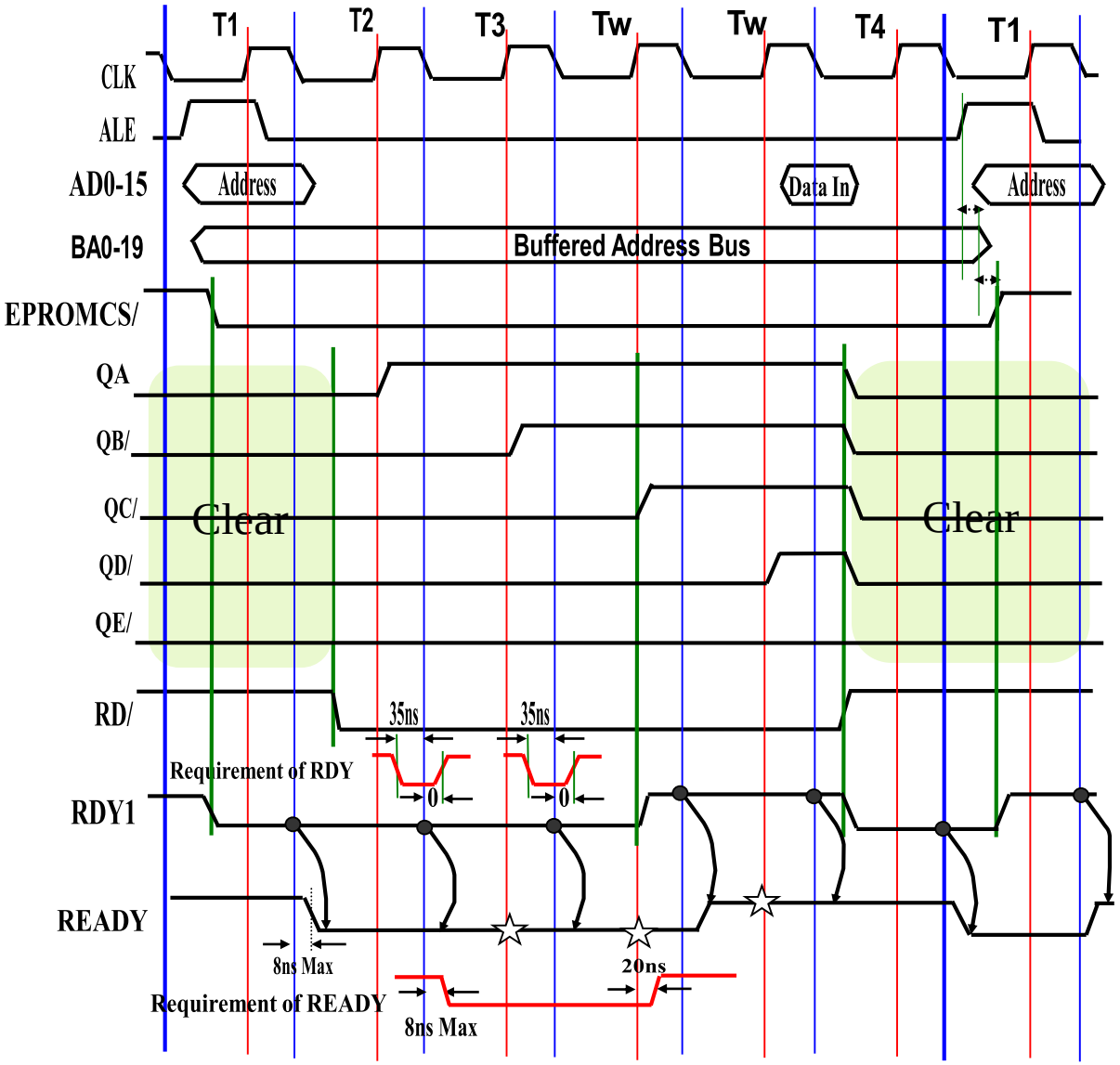
Minimum Mode 8088 System with Wait State Generator Circuit



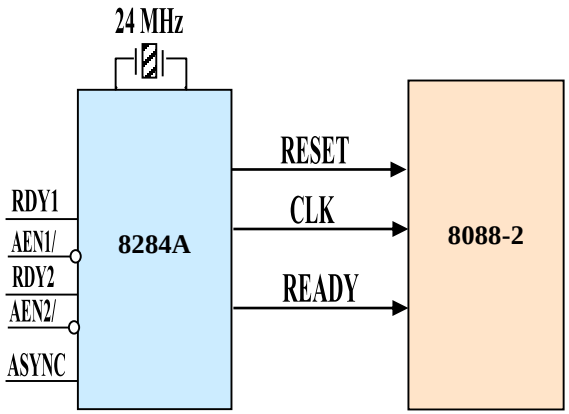
Timing Waveforms of 8088/8086 Bus Cycle with One Wait State



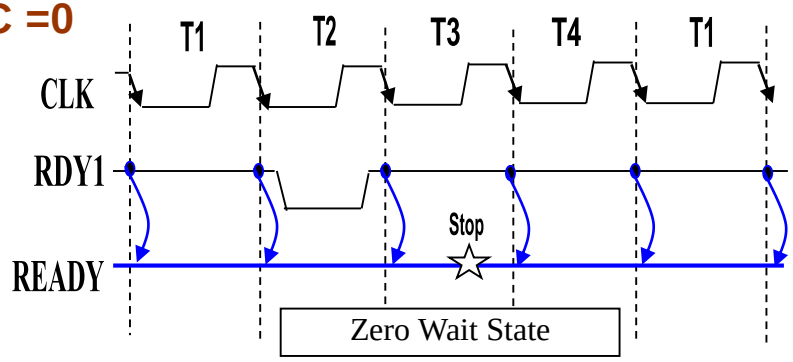
Timing Waveforms of 8088/8086 Bus Cycle with Two Wait States

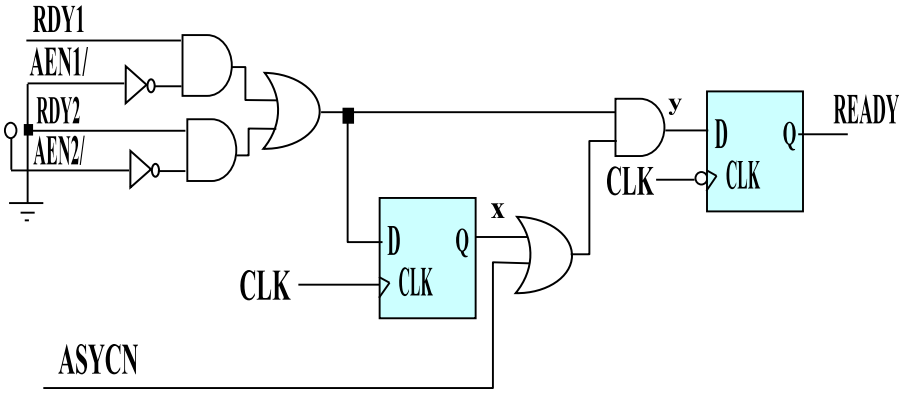


ASYNC Signal

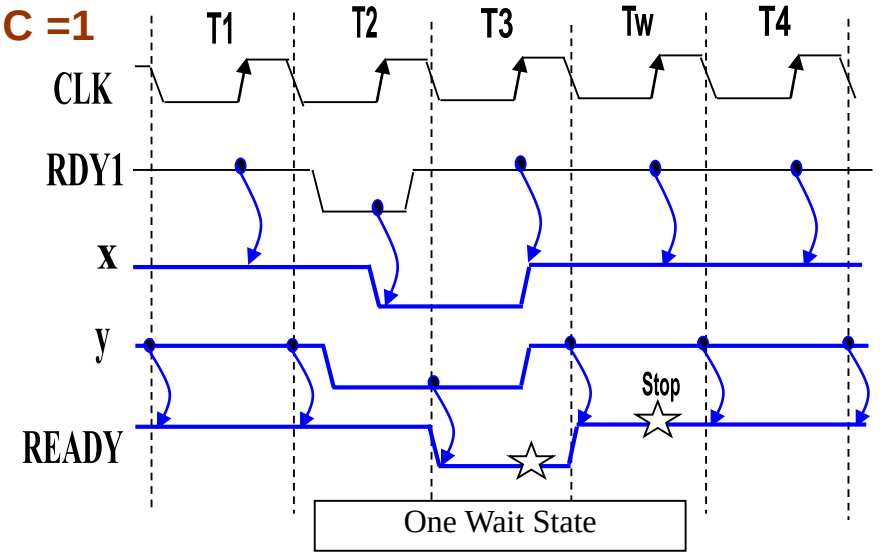


$\overline{\text{ASYNC}}$ =0

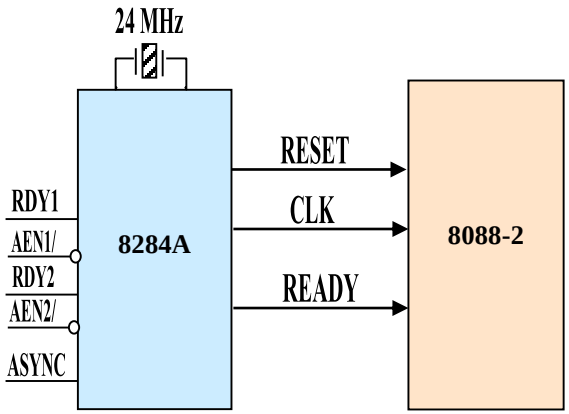




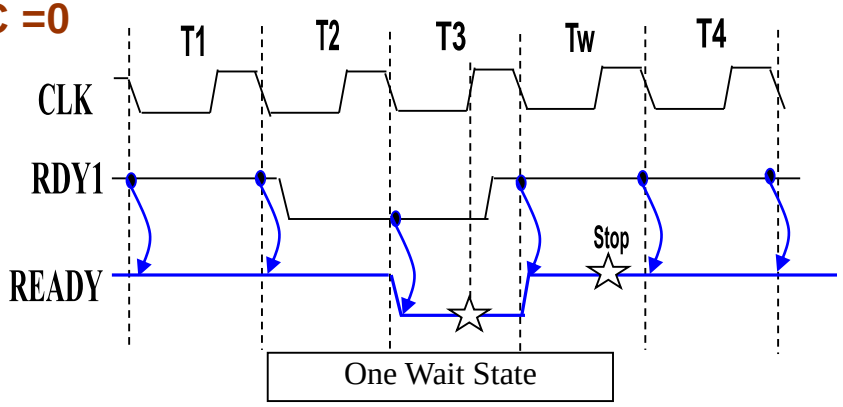
$\overline{\text{ASYNC}}$ =1

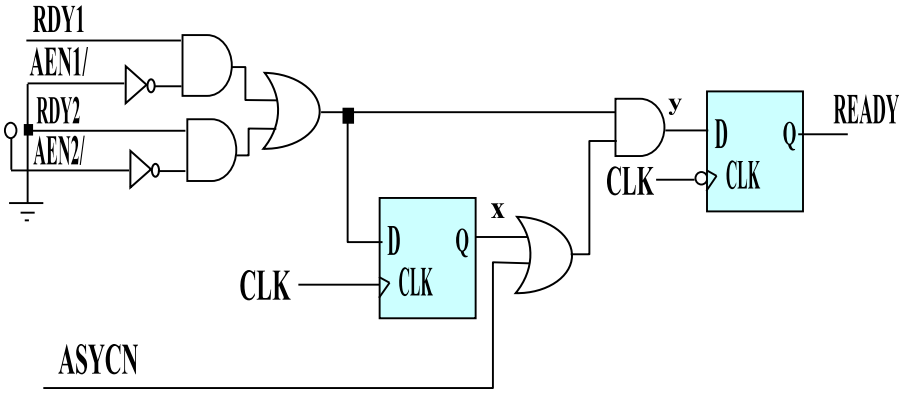


ASYNC Signal

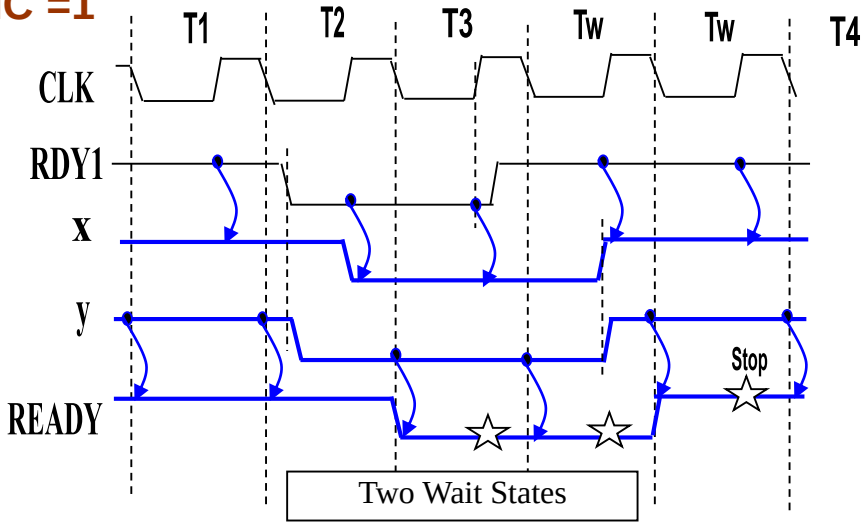


$\overline{\text{ASYNC}}$ =0

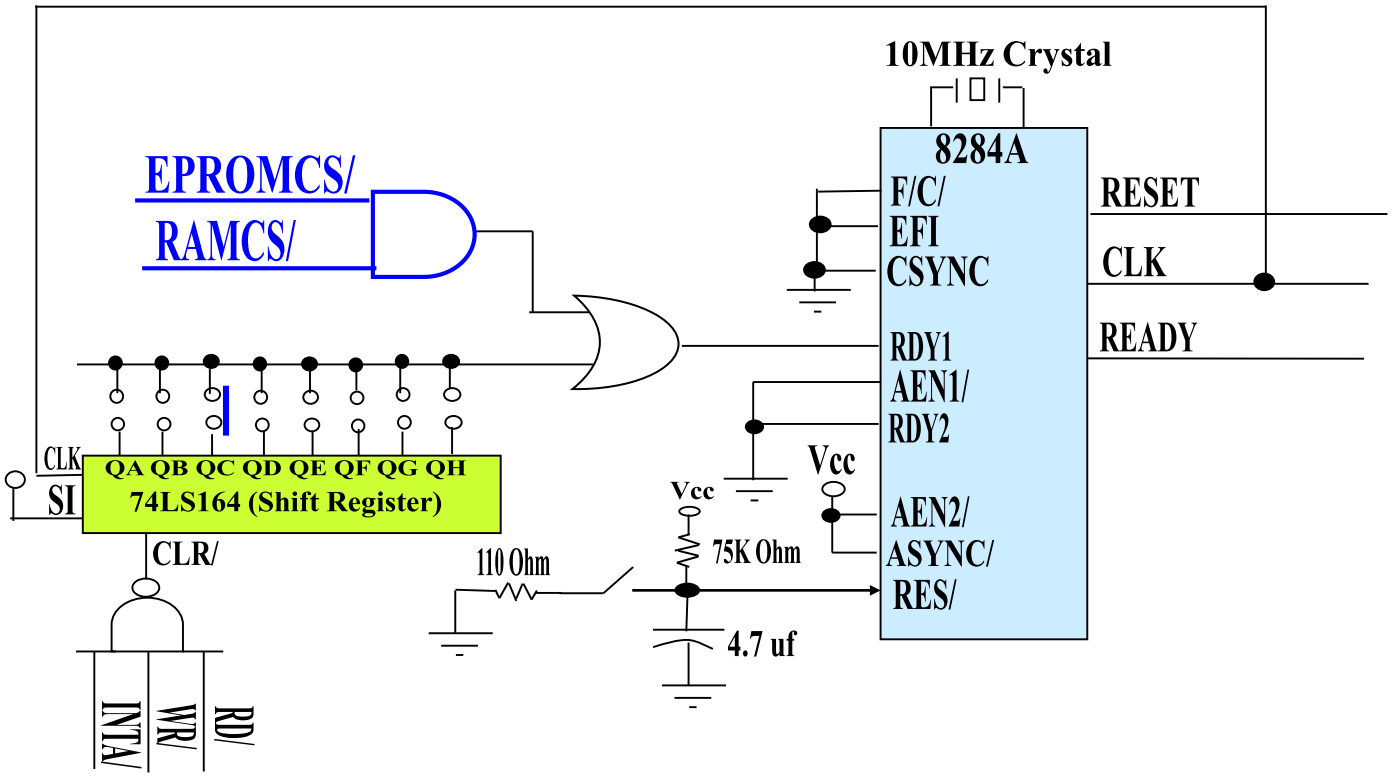




$\overline{\text{ASYNC}}$ =1

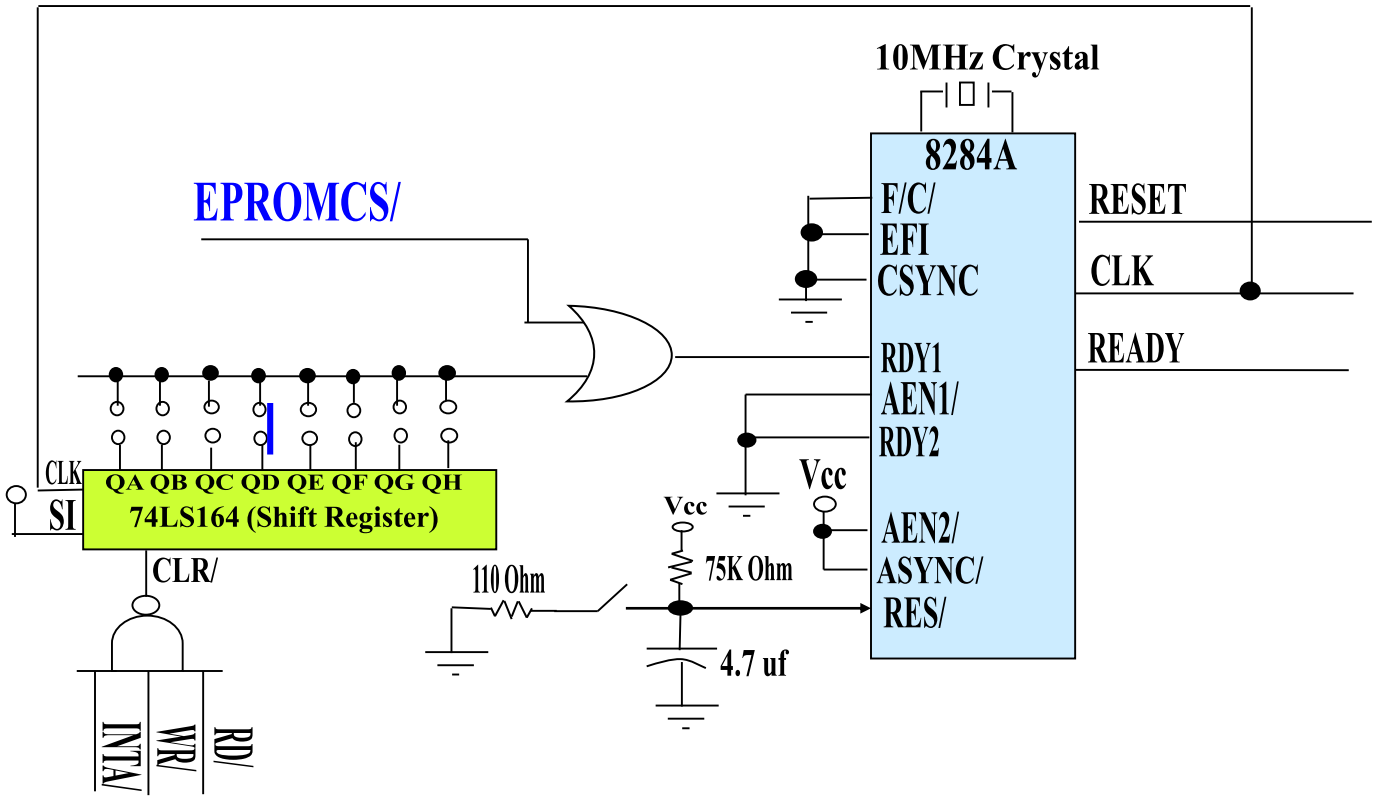


Examples



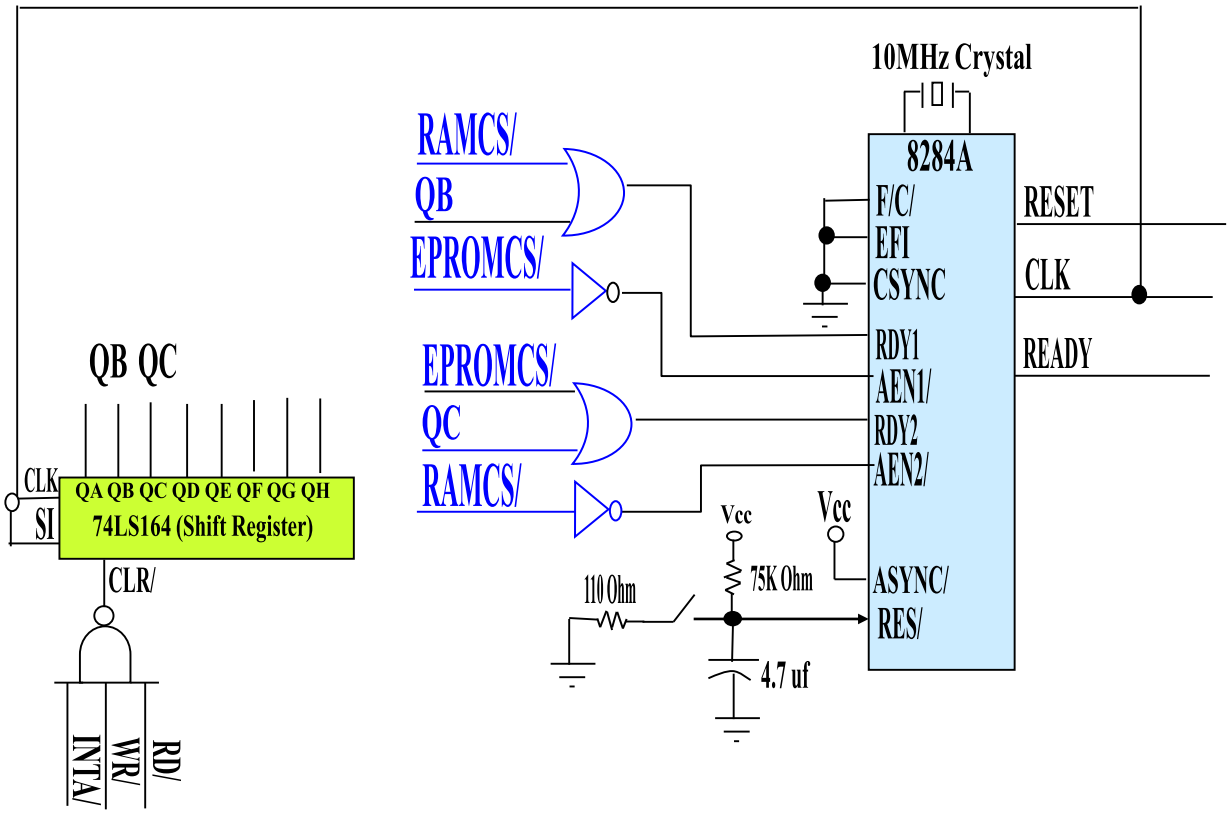
RAM and EPROM require 2 wait states

Examples



RAM requires 0 wait state and EPROM requires 3 wait states

Examples



RAM requires 1 wait state and EPROM requires 2 wait states