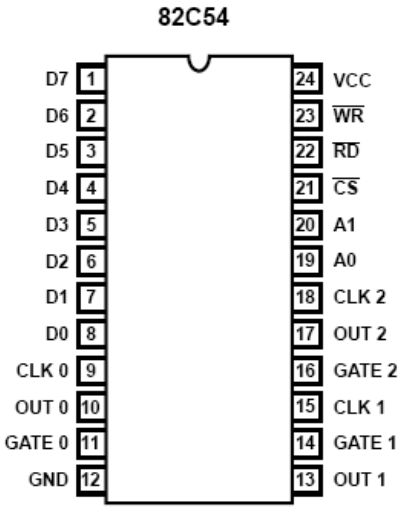
Programmable Interval Timer - 8254

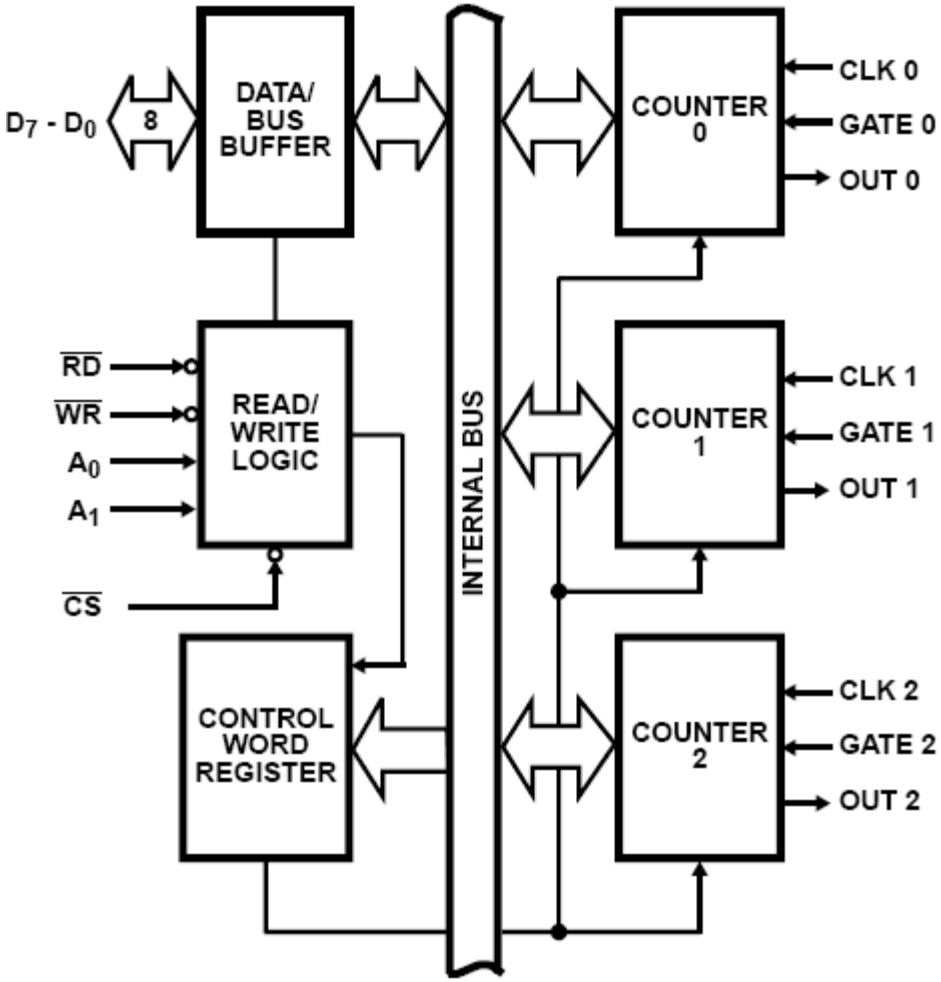
CEN433

King Saud University

Dr. Mohammed Amer Arafah

Functional Diagram





8254: Pin Description

SYMBOL	DIP PIN NUMBER	TYPE	DEFINITION
D7 - D0	1 - 8	I/O	DATA: Bi-directional three-state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
OUT 1	13	O	OUT 1: Output of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
OUT 2	17	O	OUT 2: Output of Counter 2.
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
A0, A1	19 - 20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus.
$\overline{CS}$	21	I	CHIP SELECT: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	READ: This input is low during CPU read operations.
$\overline{WR}$	23	I	WRITE: This input is low during CPU write operations.
V_{CC}	24		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins VCC and GND is recommended for decoupling.

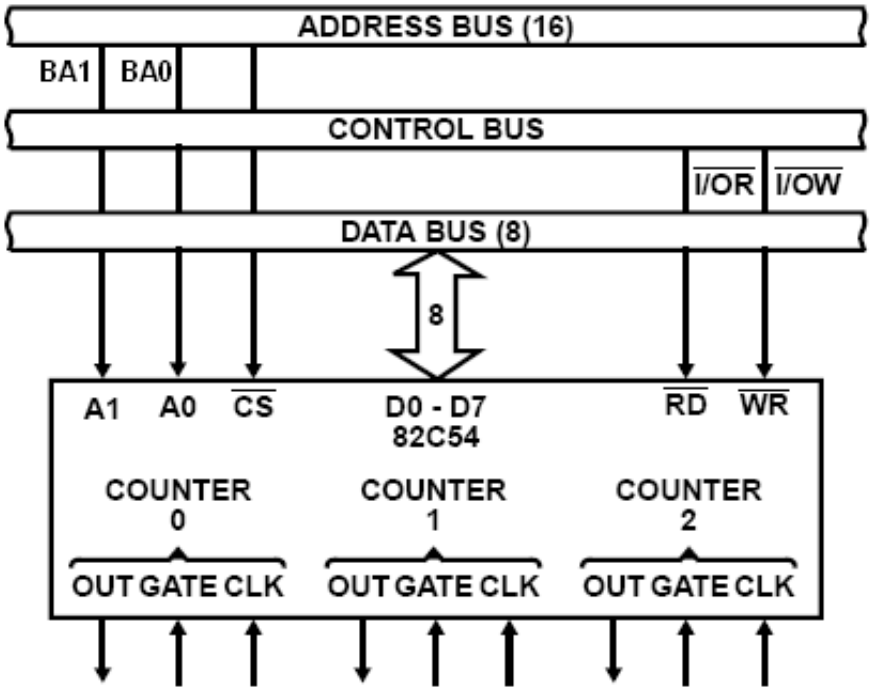
A1	A0	SELECTS
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

8254: Read/Write Operations Summary

A1	A0	SELECTS
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (Three-State)
1	X	X	X	X	No-Operation (Three-State)
0	1	1	X	X	No-Operation (Three-State)

8254 System Interface



Control Word Format

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - Read/Write

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal

0	Binary Counter 16-bit
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

Possible Programming Sequence

	A1	A0
Control Word - Counter 0	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
Control Word - Counter 1	1	1
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0

	A1	A0
Control Word - Counter 0	1	1
Control Word - Counter 1	1	1
Control Word - Counter 2	1	1
LSB of Count - Counter 2	1	0
LSB of Count - Counter 1	0	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0
MSB of Count - Counter 1	0	1
MSB of Count - Counter 2	1	0

	A1	A0
Control Word - Counter 2	1	1
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 2	1	0
LSB of Count - Counter 1	0	1
MSB of Count - Counter 1	0	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 0	0	0

	A1	A0
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of Count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of Count - Counter 0	0	0
MSB of Count - Counter 1	0	1
LSB of Count - Counter 2	1	0
MSB of Count - Counter 0	0	0
MSB of Count - Counter 2	1	0

Write Operations

- The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:
  1. For Each Counter, the Control Word must be written before the initial count is written.
  2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Programming the 8254

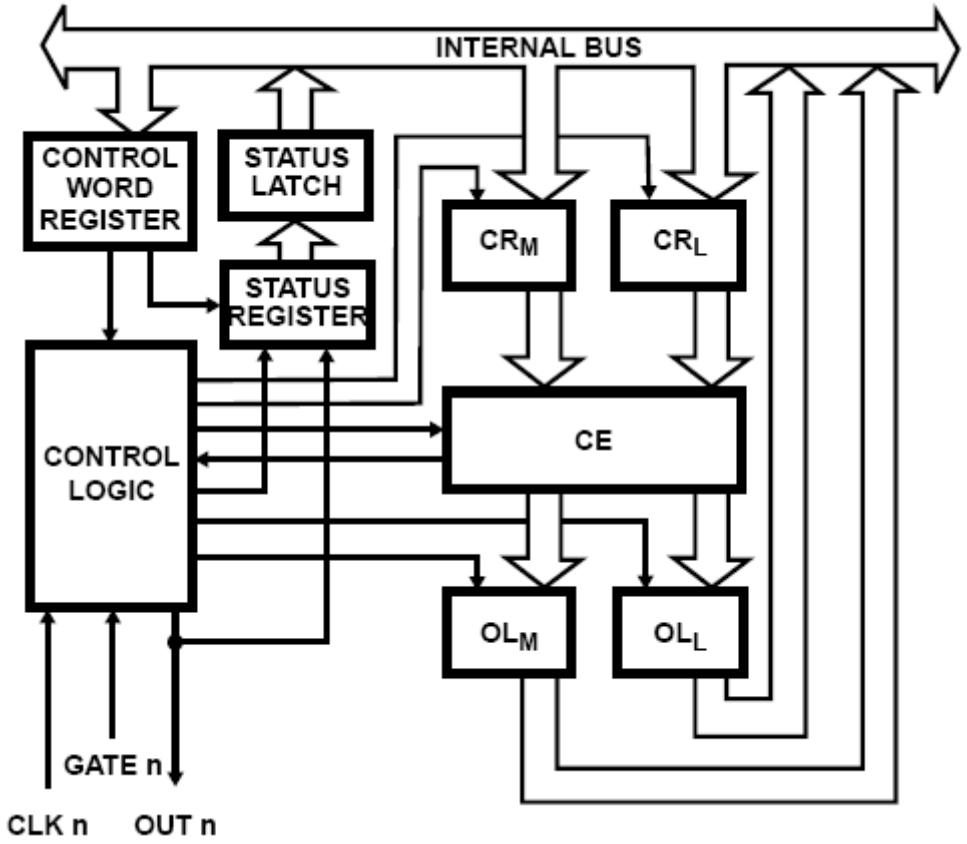
```
MOV     DX, TCW
MOV     AL, 00110110B       ; Control Word of Counter0: LSB then MSB, Mode 3, Binary
OUT     DX, AL
MOV     DX, TCW
MOV     AL, 01110110B       ; Control Word of Counter1: LSB then MSB, Mode 3, Binary
OUT     DX, AL
MOV     DX, TCW
MOV     AL, 10110110B       ; Control Word of Counter2: LSB then MSB, Mode 3, Binary
OUT     DX, AL

; Initialize value of Counter 0
MOV     DX, COUNTER0
MOV     AL, Counter0_LSB    ;LSB of Counter 0
OUT     DX, AL
MOV     AL, Counter0_MSB    ;MSB of Counter 0
OUT     DX, AL

; Initialize value of Counter 1
MOV     DX, COUNTER1
MOV     AL, Counter1_LSB    ;LSB of Counter 1
OUT     DX, AL
MOV     AL, Counter1_MSB    ;MSB of Counter 1
OUT     DX, AL

; Initialize value of Counter 2
MOV     DX, COUNTER2
MOV     AL, Counter2_LSB    ;LSB of Counter 2
OUT     DX, AL
MOV     AL, Counter2_MSB    ;MSB of Counter 2
OUT     DX, AL
```

Counter Internal Block Diagram



8254: Read Operation

- There are three possible methods for reading a counter:
  - **A Simple Read Operation.**
  - **The Counter Latch Command.**
  - **The Read-Back Command.**

8254: Counter Latch Command

- This Counter Latch Command is written to the **Control Word Register**, which is selected when **A1 A0** = 11.
- The **SC1** and **SC0** bits select one of the three counters.
- **D5 D4** = 00 designates **Counter Latch Command**.
- The selected counter's **output latch** (OL) latches the count at the time Counter Latch Command is received.
- The count is held in the OL until it is read by the CPU (or until the counter is reprogrammed).
- The count is then unlatched automatically and the OL returns to "following" the **counting element** (CE).
- If the counter is latched, and then latched again before the count is read, the second **Counter Latch Command** is ignored.

8254: Counter Latch Command

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	COUNTER
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5, D4 - 00 designates Counter Latch Command, X - Don't Care.
NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

8254: Counter Latch Command

```
; Latching Counter 0
        MOV     DX, TIMER_PORT3
        MOV     AL, 00000000B           ; Count Latched for Counter 0
        OUT     DX, AL
; Reading Counter 0
        MOV     DX, TIMER_PORT0
        IN      AL, DX
```

8254: Read-Back Command

- The **Read-Back Command** allows the user to check the count value, programmed mode, and current states of the **OUT** pin and **NULL Count** flag of the selected counter(s).
- The **Read-Back Command** is written into the **Control Word Register**.
- The **Read-Back Command** may be used to latch multiple counter output latches(s) by setting **COUNT/** bit **D5** = 0 and selecting the desired counters.
- A single **Read-Back Command** is equivalent to several **Count Latch Commands**.
- Each Counter's latched count is held in the OL until it is read by CPU (or the counter is reprogrammed).
- The counter is automatically unlatched when read, but other counters remain latched until they are read.

8254: Read-Back Command

- If multiple **Read-Back Command** are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first **Read-Back Command** was issued.
- The **Read-Back Command** may also be used to latch status information of selected counter(s) by setting **STATUS/** bit D4 = 0.
- Status must be latched to be read; status of a counter is accessed by a read from that counter.
- If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored.
- If both count and status of a counter are latched, the first read operation of that counter will return latched status. The next one or two reads return latched count.

8254: Read-Back Command

A0, A1 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D5: 0 = Latch count of selected Counter (s)
D4: 0 = Latch status of selected Counter(s)
D3: 1 = Select Counter 2
D2: 1 = Select Counter 1
D1: 1 = Select Counter 0
D0: Reserved for future expansion; Must be 0

Read-Back Command Example:

COMMANDS								DESCRIPTION	RESULT
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read-Back Count and Status of Counter 0	Count and Status Latched for Counter 0
1	1	1	0	0	1	0	0	Read-Back Status of Counter 1	Status Latched for Counter 1
1	1	1	0	1	1	0	0	Read-Back Status of Counters 2, 1	Status Latched for Counter 2, But Not Counter 1
1	1	0	1	1	0	0	0	Read-Back Count of Counter 2	Count Latched for Counter 2
1	1	0	0	0	1	0	0	Read-Back Count and Status of Counter 1	Count Latched for Counter 1, But Not Status
1	1	1	0	0	0	1	0	Read-Back Status of Counter 1	Command Ignored, Status Already Latched for Counter 1

8254: Read-Back Command

```
; Count and Status Latched for Counter 0
        MOV     DX, TIMER_PORT3
        MOV     AL, 11000010B           ; Count Latched for Counter 0
        OUT     DX, AL
; Reading the Latched Status for Counter 0
        MOV     DX, TIMER_PORT0
        IN      AL, DX                  ; Reading Status
        MOV     AH, AL
; Reading the Latched Count for Counter 0
        IN      AL, DX                  ; Reading LSB of Counter 0
        MOV     BL, AL
        IN      AL, DX                  ; Reading MSB of Counter 0
        MOV     BH, AL
```

8254: Status Byte

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7: 1 = Out pin is 1
0 = Out pin is 0
D6: 1 = Null count
0 = Count available for reading
D5 - D0 = Counter programmed mode (See Control Word Formats)

THIS ACTION:	CAUSES:
A. Write to the control word register:(1)	Null Count = 1
B. Write to the count register (CR):(2)	Null Count = 1
C. New count is loaded into CE (CR - CE)	Null Count = 0

(1) Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

(2) If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

Modes of Operation

Mode 0: Interrupt on Terminal Count

Mode 1: Hardware Retriggerable One-Shot

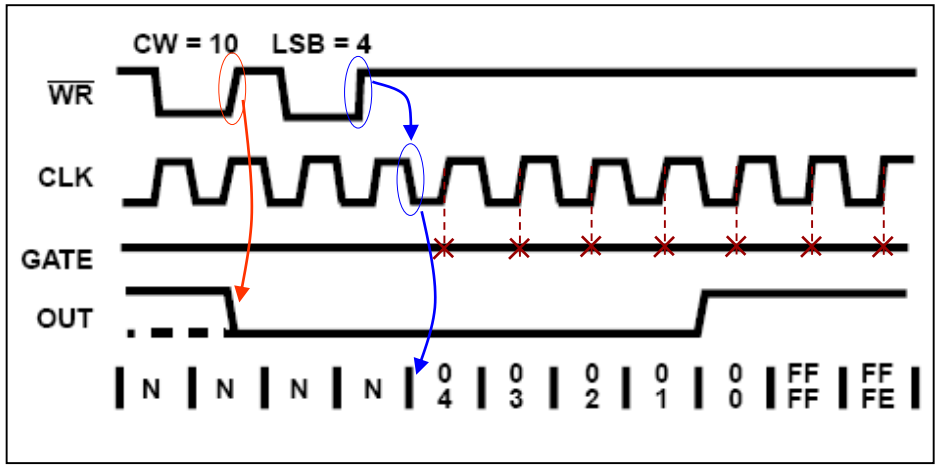
Mode 2: Rate Generator

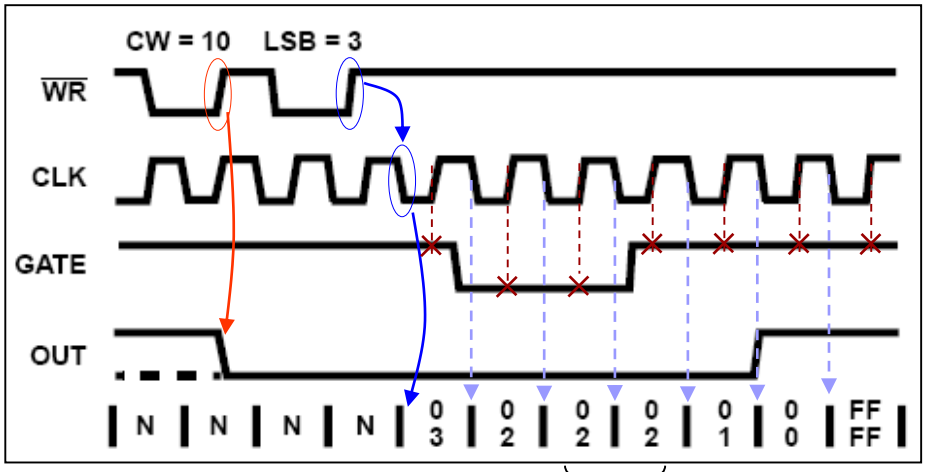
Mode 3: Square Wave Mode

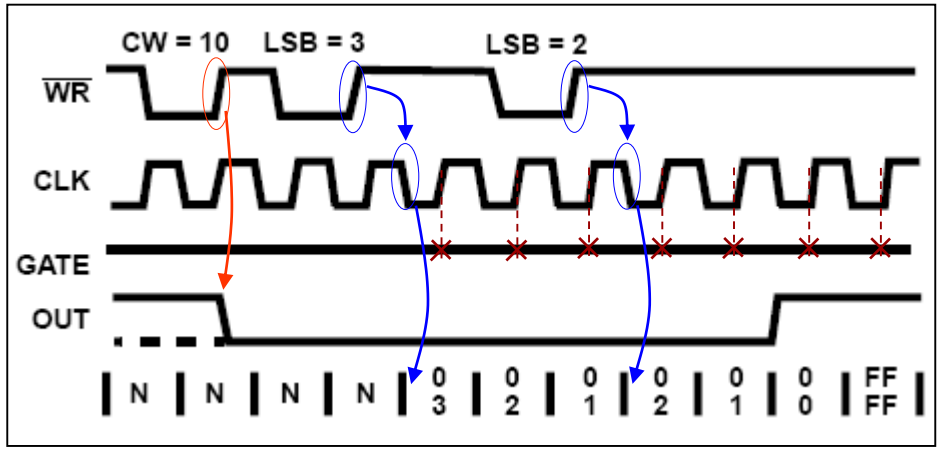
Mode 4: Software Triggered Mode

Mode 5: Hardware Triggered Mode

Mode 0: Interrupt on Terminal Count

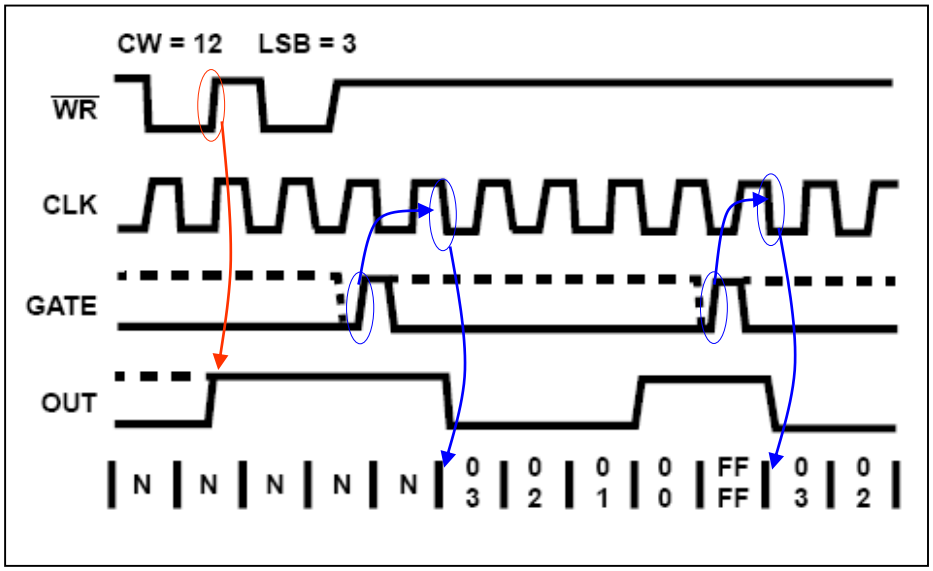


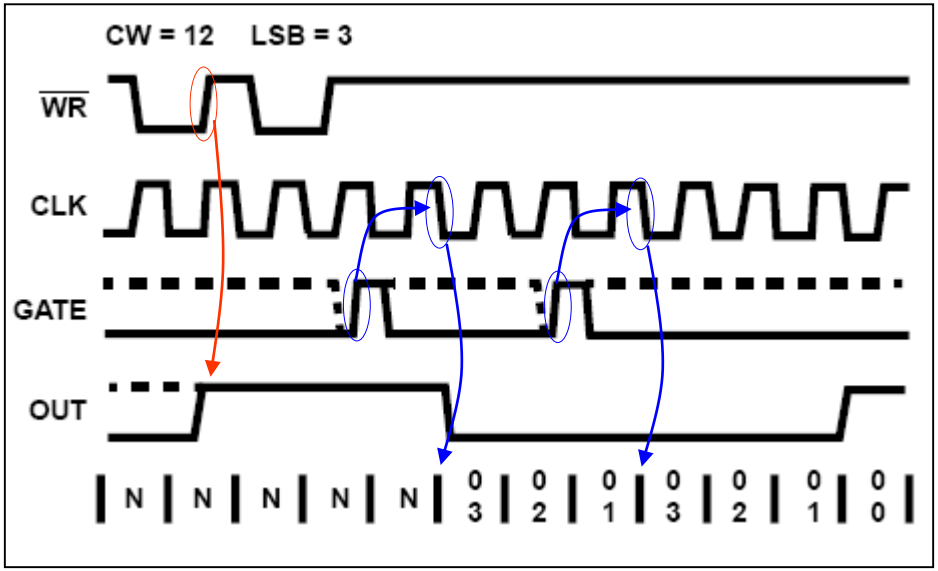


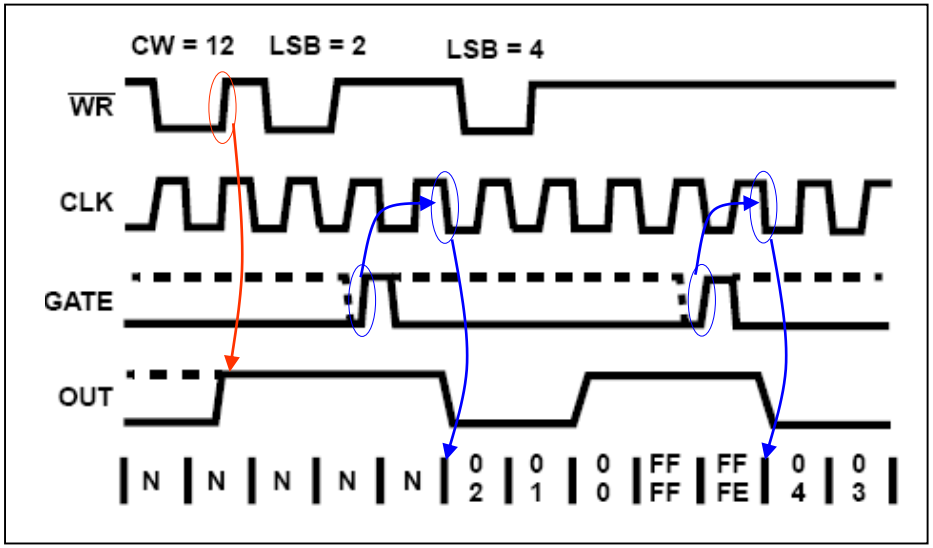


- At the rising edge of WR/ (Control Word), OUT = low.
- At the first falling edge of CLK after the rising edge of WR/ (LSB), CR→CE.
- GATE is level sensitive.
- GATE is sampled at the rising edge of CLK.
- Decrement the counter at the falling edge, if the sample of GATE is high. Otherwise, freeze.

Mode 1: Hardware Retriggerable One-Shot

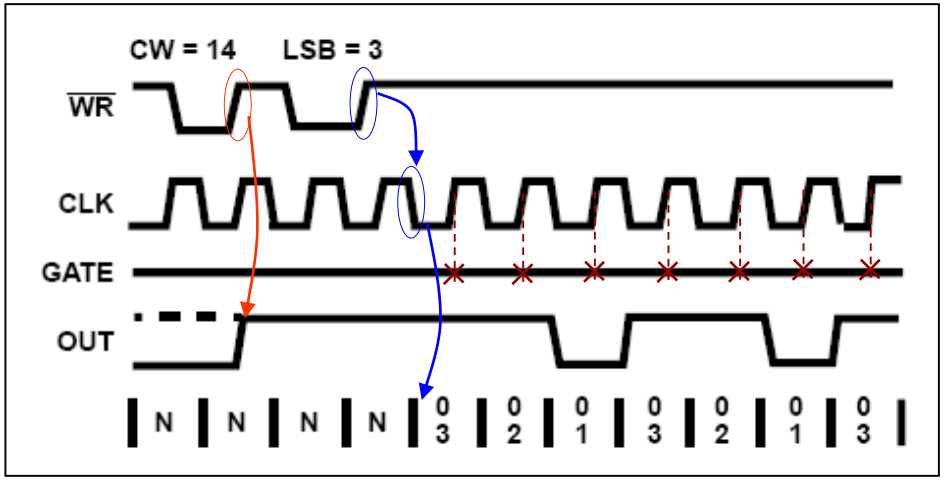


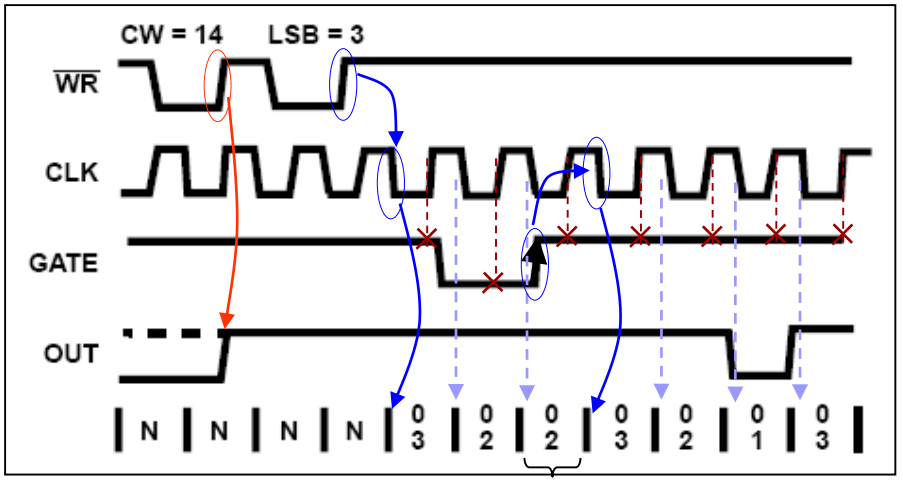


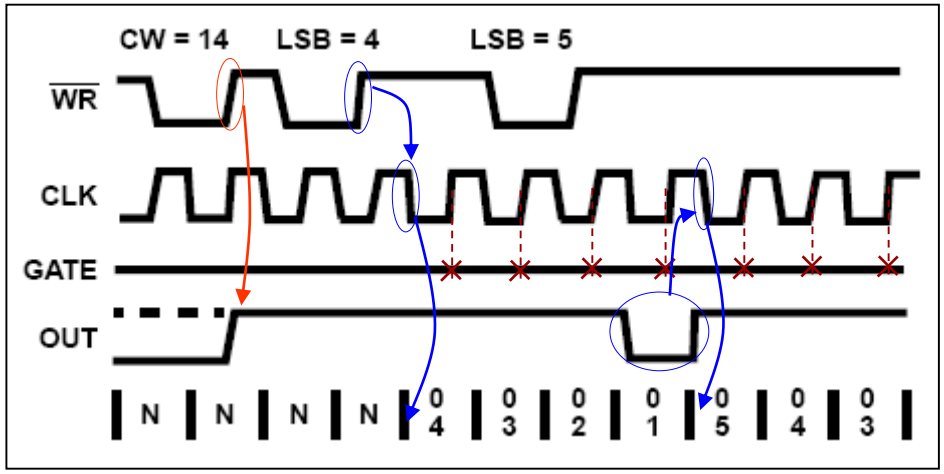


- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of GATE, CR→CE.
- At the first falling edge of CLK after the rising edge of GATE, reinitialize CE with the last value written to CR.

Mode 2: Rate Generator

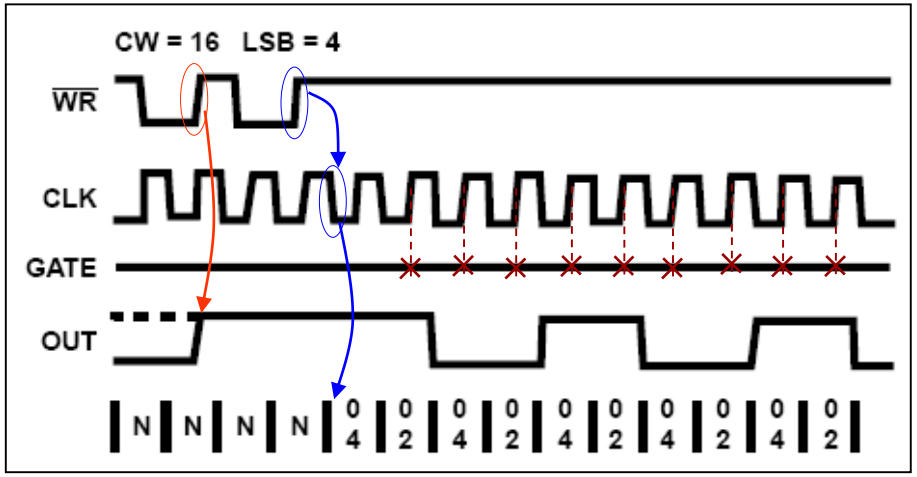


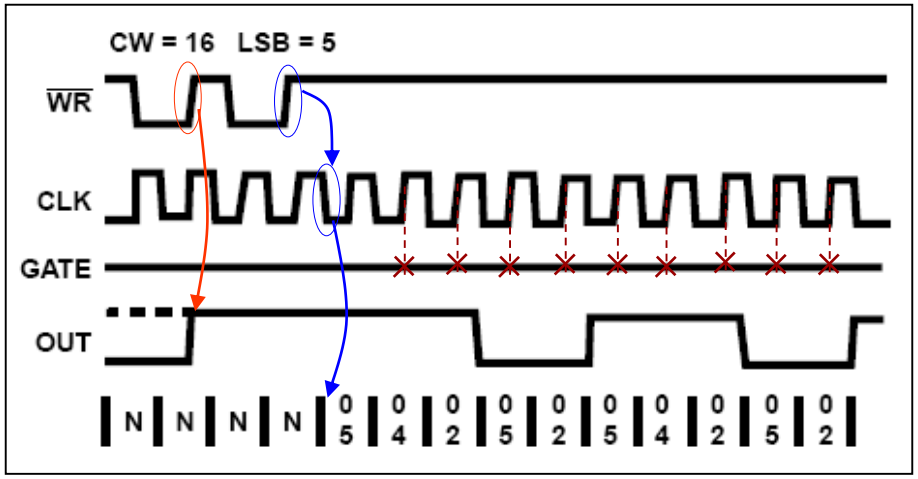


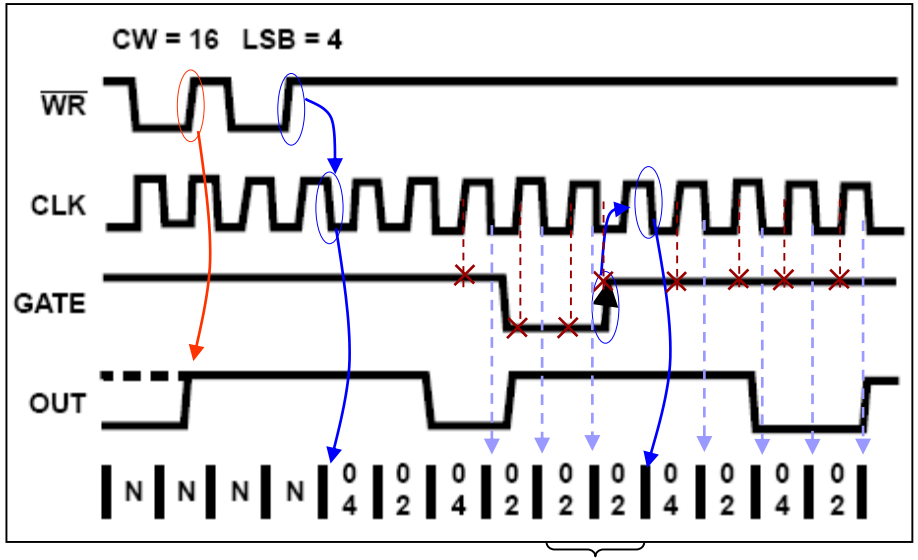


- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of WR/ (LSB), CR→CE.
- When counter reaches to value 1, it is reloaded with the value of CR at the next falling edge of CLK.
- GATE is sampled at the rising edge of CLK.
- Decrement the counter at the falling edge, if the sample of GATE is high. Otherwise, freeze.
- At the first falling edge of CLK after the rising edge of the GATE, reinitialize CE.

Mode 3: Square Wave Mode

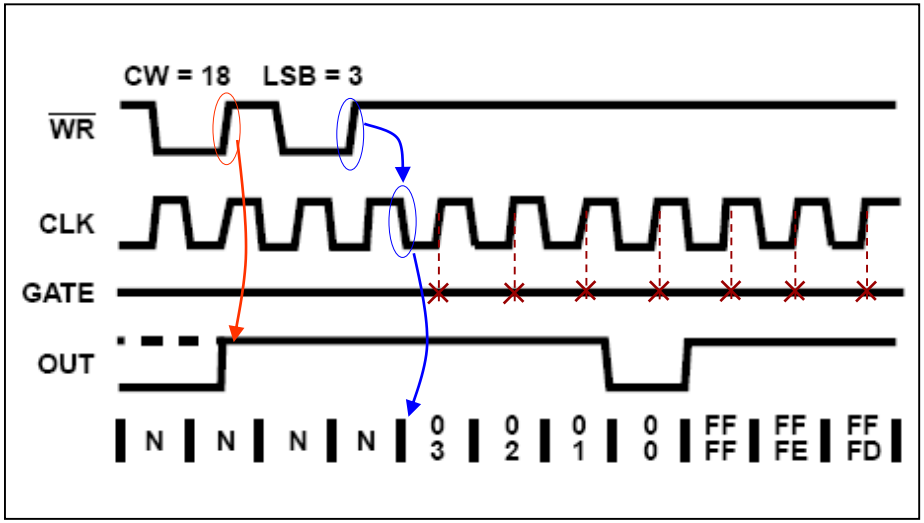


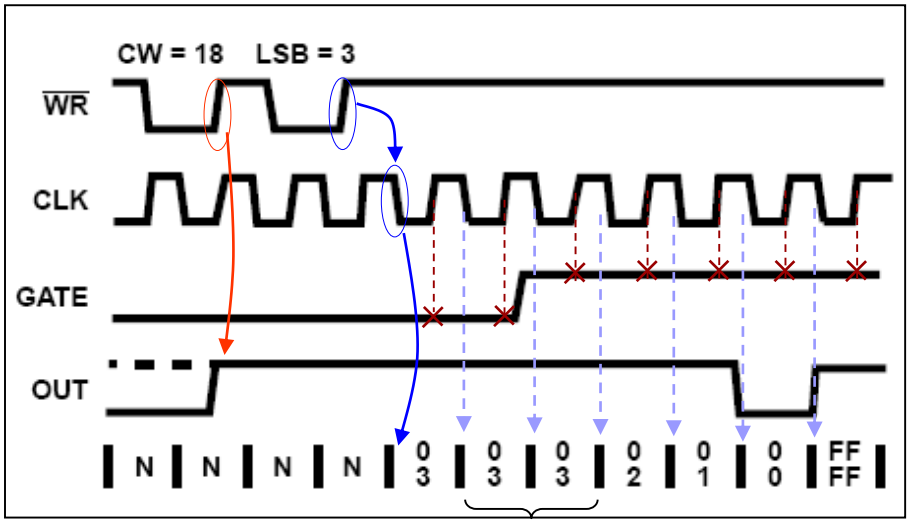


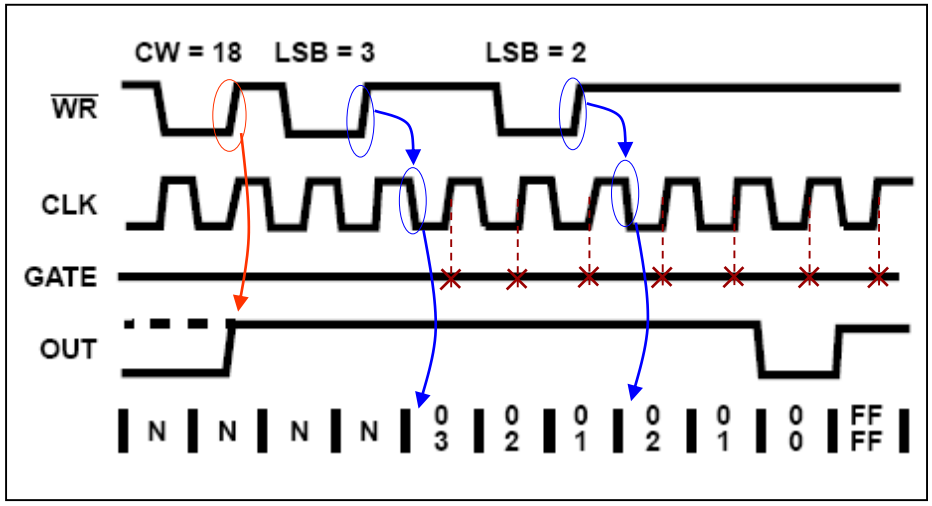


- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of WR/ (LSB), CR→CE.
- GATE is sampled at the rising edge of CLK.
- At the first falling edge of CLK after the rising edge of the GATE, reinitialize CE.

Mode 4: Software Triggered Mode

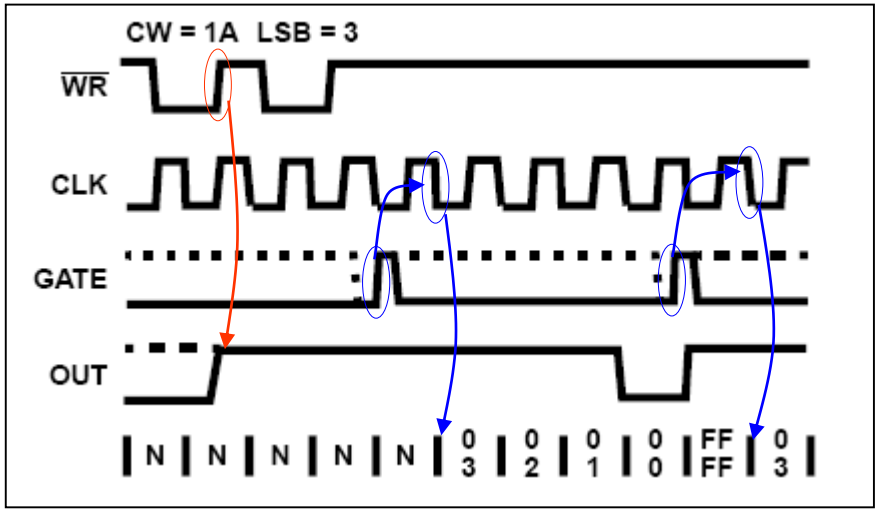


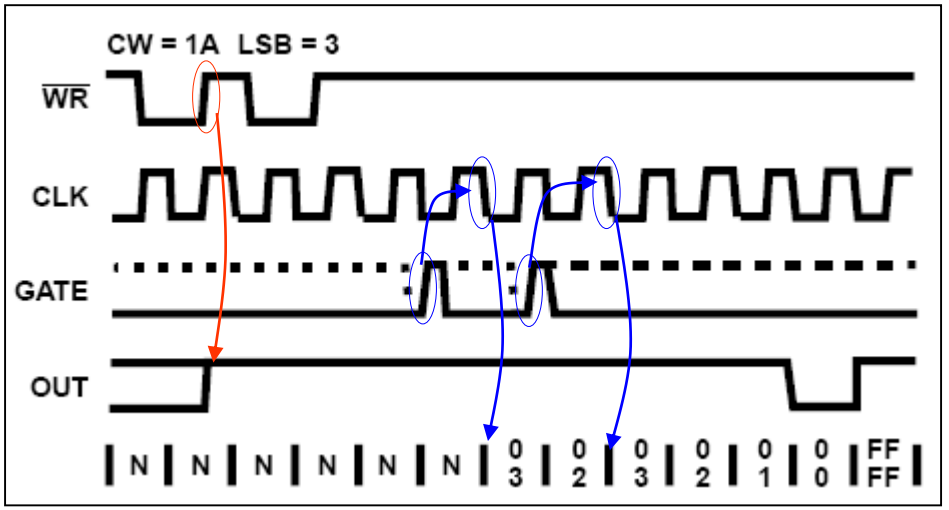


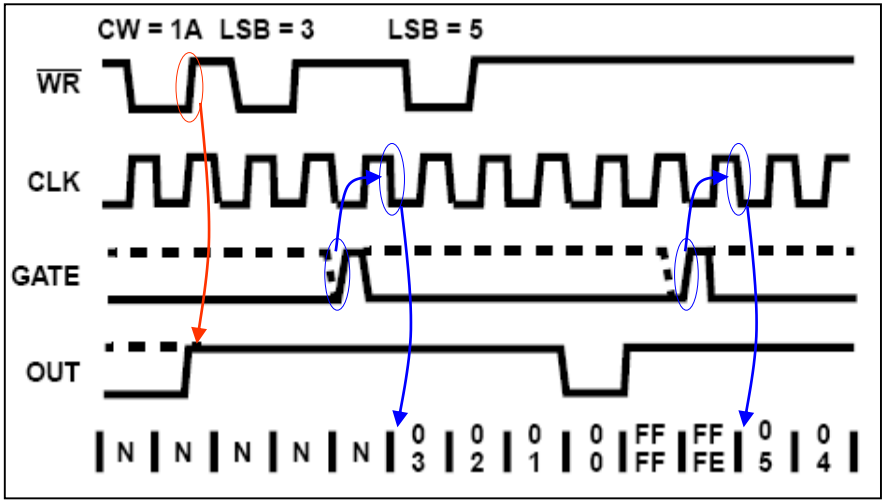


- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of WR/ (LSB), CR→CE.
- GATE is level sensitive.
- GATE is sampled at the rising edge of CLK.
- Decrement the counter at the falling edge, if the sample of GATE is high. Otherwise, freeze.
- When counter reaches to zero, it wraps around to the highest value.

Mode 5: Hardware Triggered Mode







- At the rising edge of WR/ (Control Word), OUT = high.
- At the first falling edge of CLK after the rising edge of GATE, CR→CE.
- At the first falling edge of CLK after the rising edge of GATE, reinitialize CE with the last value written to CR.
- When counter reaches to zero, it wraps around to the highest value.

Gate Pin Operations Summary

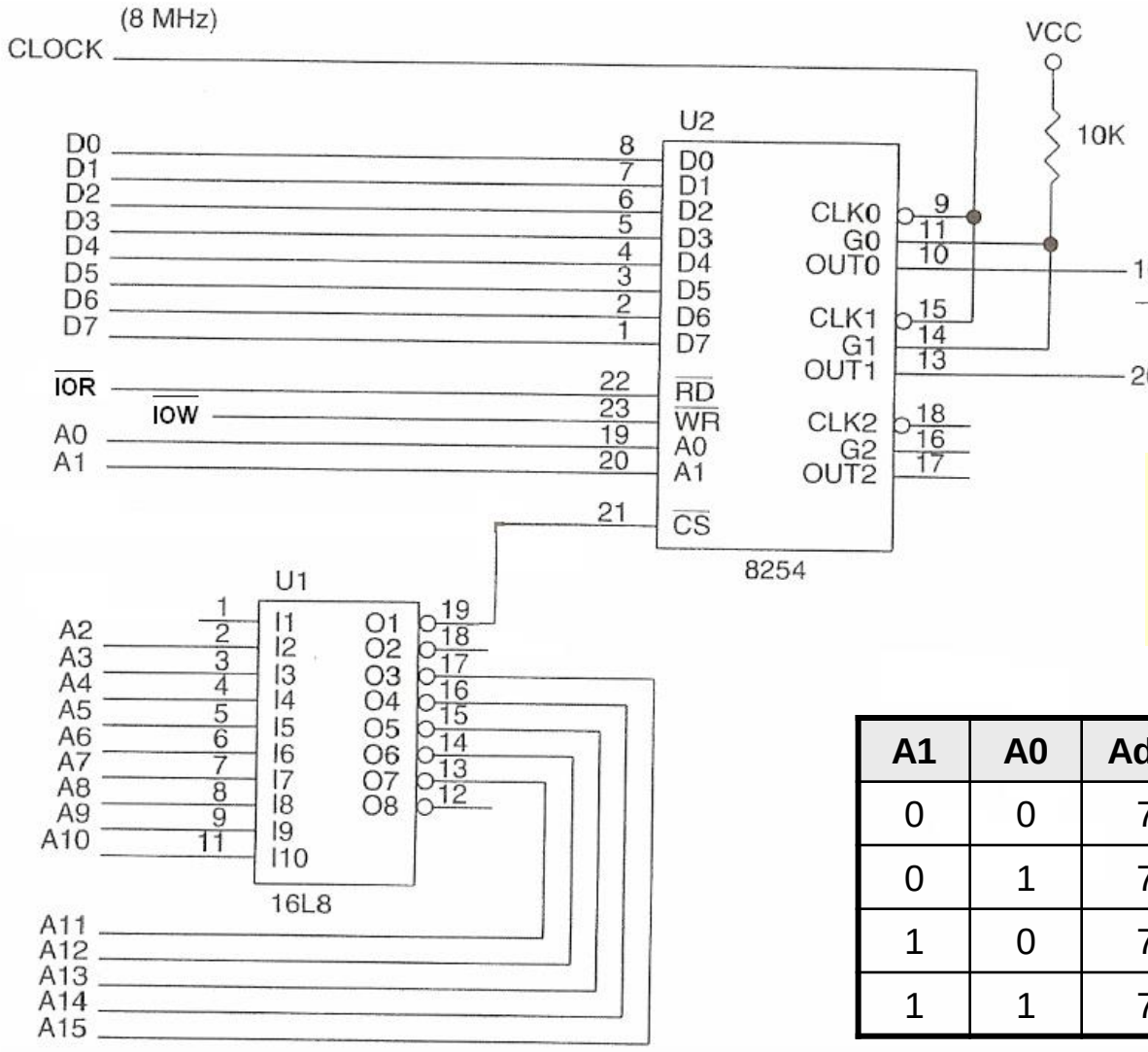
SIGNAL STATUS MODES	LOW OR GOING LOW	RISING	HIGH
0	Disables Counting	-	Enables Counting
1	-	1) Initiates Counting 2) Resets output after next clock	-
2	1) Disables counting 2) Sets output immediately high	Initiates Counting	Enables Counting
3	1) Disables counting 2) Sets output immediately high	Initiates Counting	Enables Counting
4	1) Disables Counting	-	Enables Counting
5	-	Initiates Counting	-

Minimum and Minimum Initial Counts

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Example 1



100 KHz Square Wave:
→ Mode 3
f Out = f in / n
n = 8000 KHz/100 KHz = 80d

200 KHz non-square wave:
→ Mode 2
f Out = f in / n
n = 8000 KHz/200 KHz = 40d

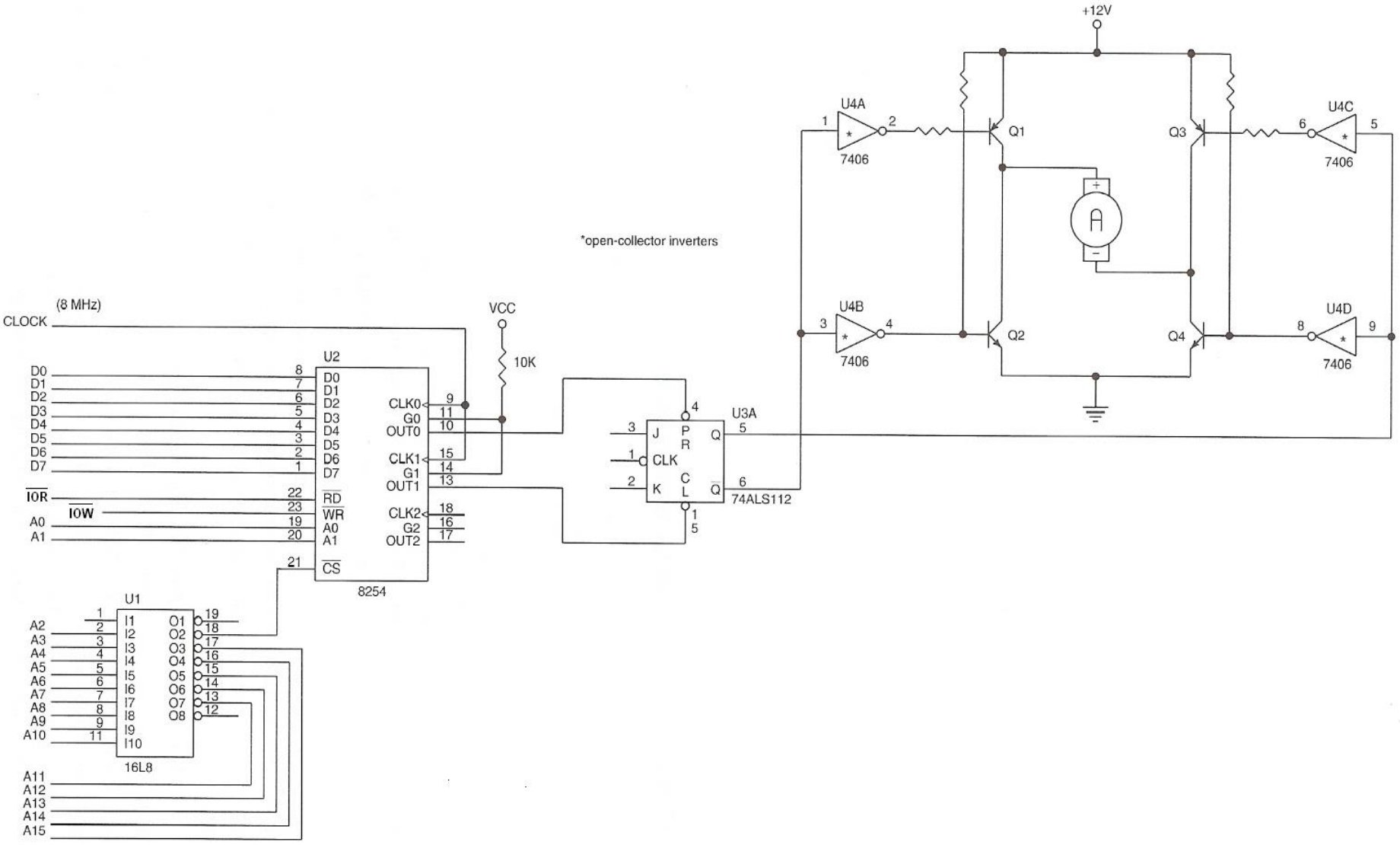
A1	A0	Address	Port
0	0	700H	Counter 0
0	1	701H	Counter 1
1	0	702H	Counter 2
1	1	703H	Control Word

Example 1

```
;A procedure that programs the 8254 timer
TIME    PROC    NEAR USES AX DX
        MOV  DX, 703H          ; Control register
        MOV  AL, 00010110B     ; Program counter 0: Mode 3, LSB only
        OUT  DX, AL
        MOV  AL, 01010100B     ; Program counter 1: Mode 2, LSB only
        OUT  DX, AL

        MOV  DX, 700H          ; Counter 0
        MOV  AL, 80            ; Load initial count 80d into counter 0
                               ; LS byte of initial count
        OUT  DX, AL
        MOV  DX, 701H          ; Counter 1
        MOV  AL, 40            ; Load initial count 40d into counter 1
        OUT  DX, AL
        MOV  AL, 0             ;Then MS byte of initial count
        OUT  DX, AL
        RET
TIME    ENDP
```

Example 2: DC Motor Speed and Direction Control-Hardware

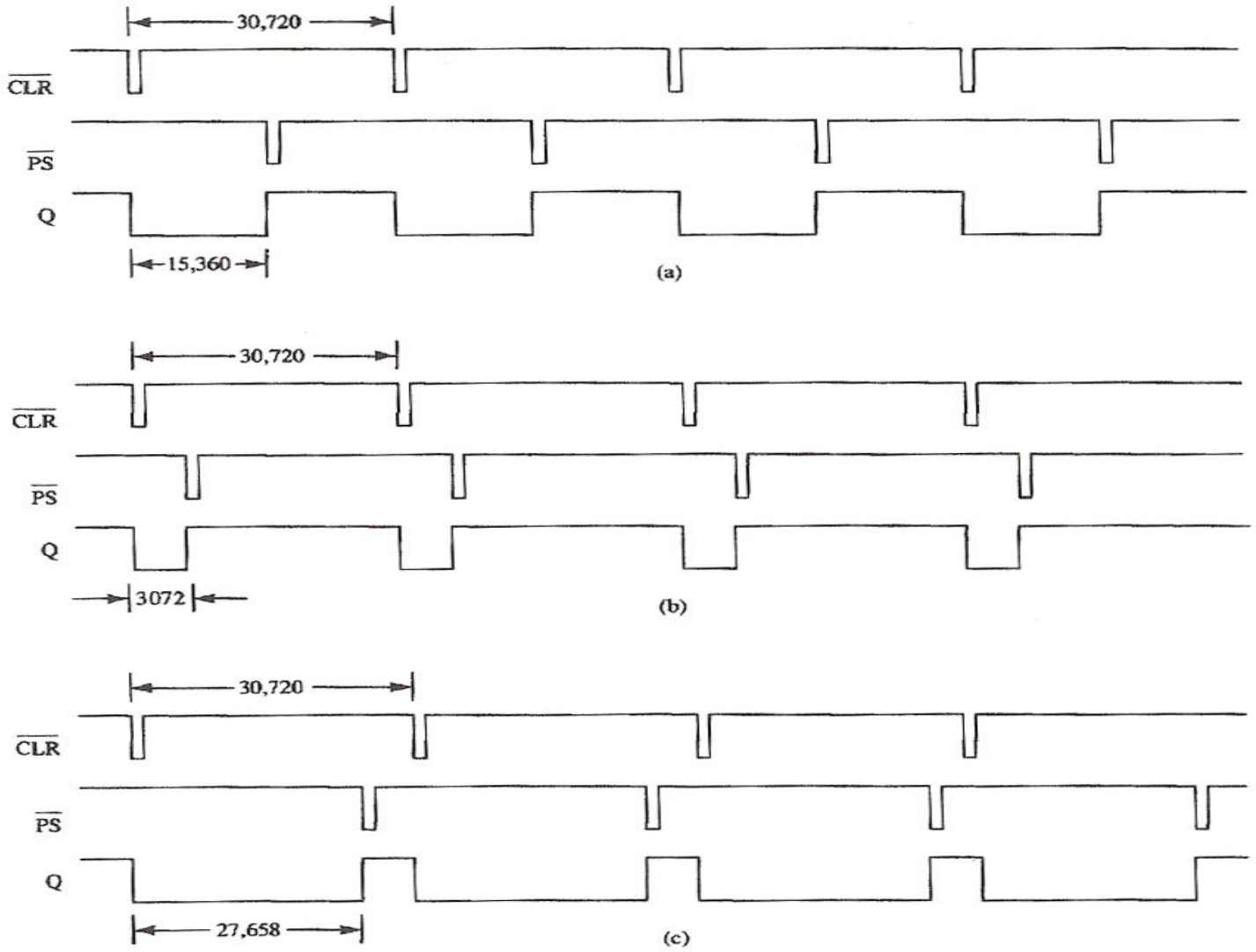


Example 2: DC Motor Speed and Direction Control - Timing

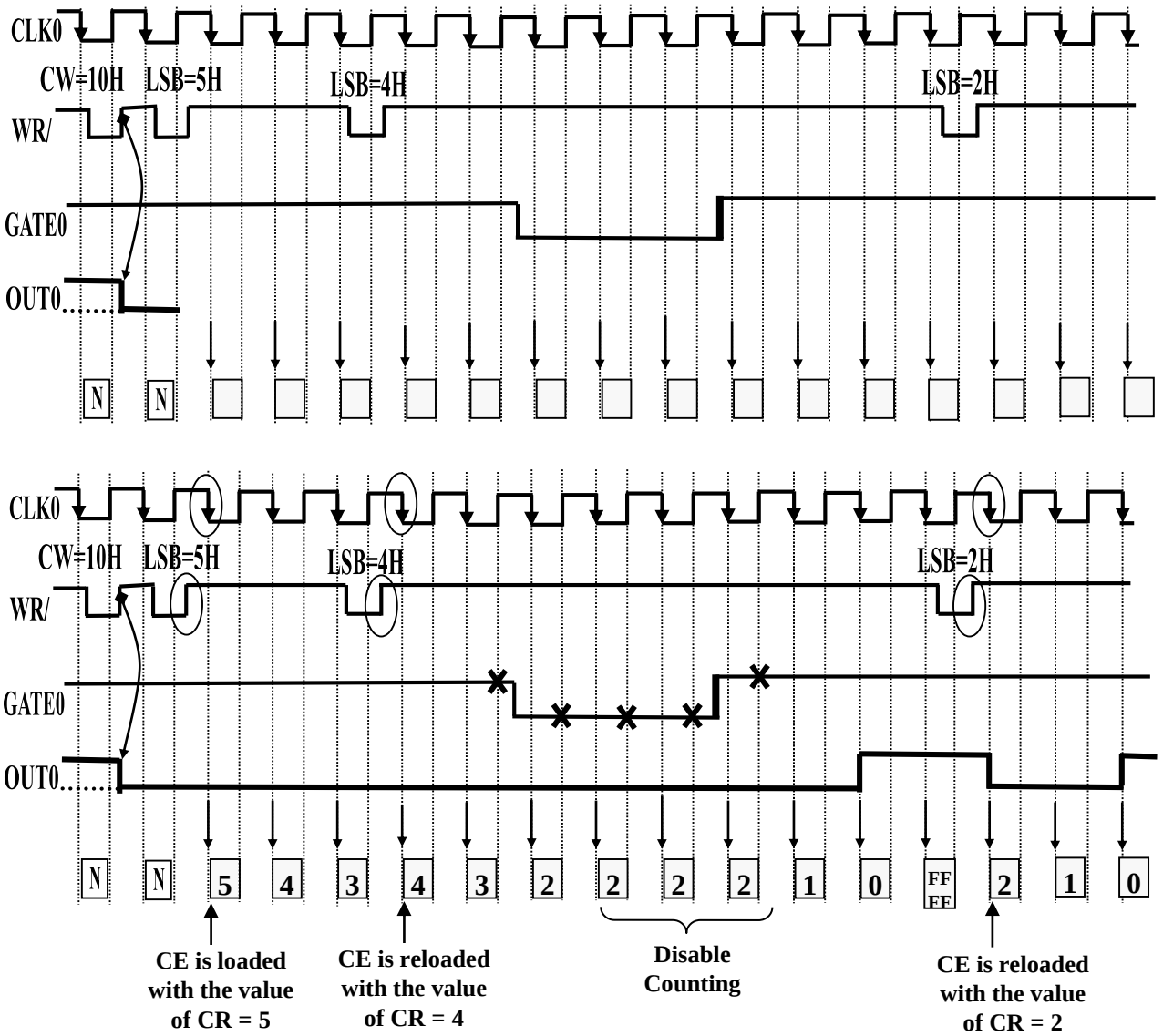
Example 2: DC Motor Speed and Direction Control-Software

```
;AH determines the speed and direction of the motor where AH is between 00H and FFH.
CNTR        EQU         703H            ; PIT Control Word
CNT0        EQU         700H
CNT1        EQU         701H
COUNT       EQU         30720
SPEED       PROC        NEAR USES BX DX AX
            MOV  BL,AH  ;calculate count corresponding to  AH: AH has speed control byte (0→128→255)
            MOV  AX,120
            MUL  BL                     ; Multiply AH (speed input) by 120
            MOV  BX,AX                  ; result in AX, save in BX (BX has AH x 120)
            MOV  AX,COUNT
            SUB  AX,BX
            MOV  BX,AX      ; Subtract from 30720, Now BX has 30720 – AH x 120 = waiting count
            MOV  DX,CNTR
            MOV  AL,00110100B           ; program control word
            OUT  DX,AL                  ; for counter 0: Binary, Mode 2, 2 bytes R/W
            MOV  AL,01110100B           ; same for counter 1
            OUT  DX,AL                  ; but do not start it yet by loading COUNT- do this after waiting time
            MOV  DX,CNT1      ; program counter 1 to generate the clear (#CLR) signal for Q (free-running)
            MOV  AX,COUNT               ;
            OUT  DX,AL                  ; LS byte of 30720 first
            MOV  AL,AH
            OUT  DX,AL                  ; then MS byte
            .REPEAT                     ; wait for counter 1 count to reach Waiting Count in BX
                        IN   AL,DX      ; Read LS byte of counter 1 (goes as AL)
                        XCHG AL,AH      ; Put it in AH
                        IN   AL,DX      ; Read MS byte of counter 1 (goes as AL)
                        XCHG AL,AH      ; swap AL and AH to put things back to order
            .UNTIL BX == AX
            MOV  DX,CNT0                ; program counter 0
            MOV  AX,COUNT               ; to generate a set (#PS) for Q (free-running) after that waiting
                                        ; delay by Counter 1. Note you also load COUNT as with Counter 1
            OUT  DX,AL                  ; Actual outputting LS byte then MS byte
            MOV  AL,AH
            OUT  DX,AL
            RET
SPEED       ENDP
```

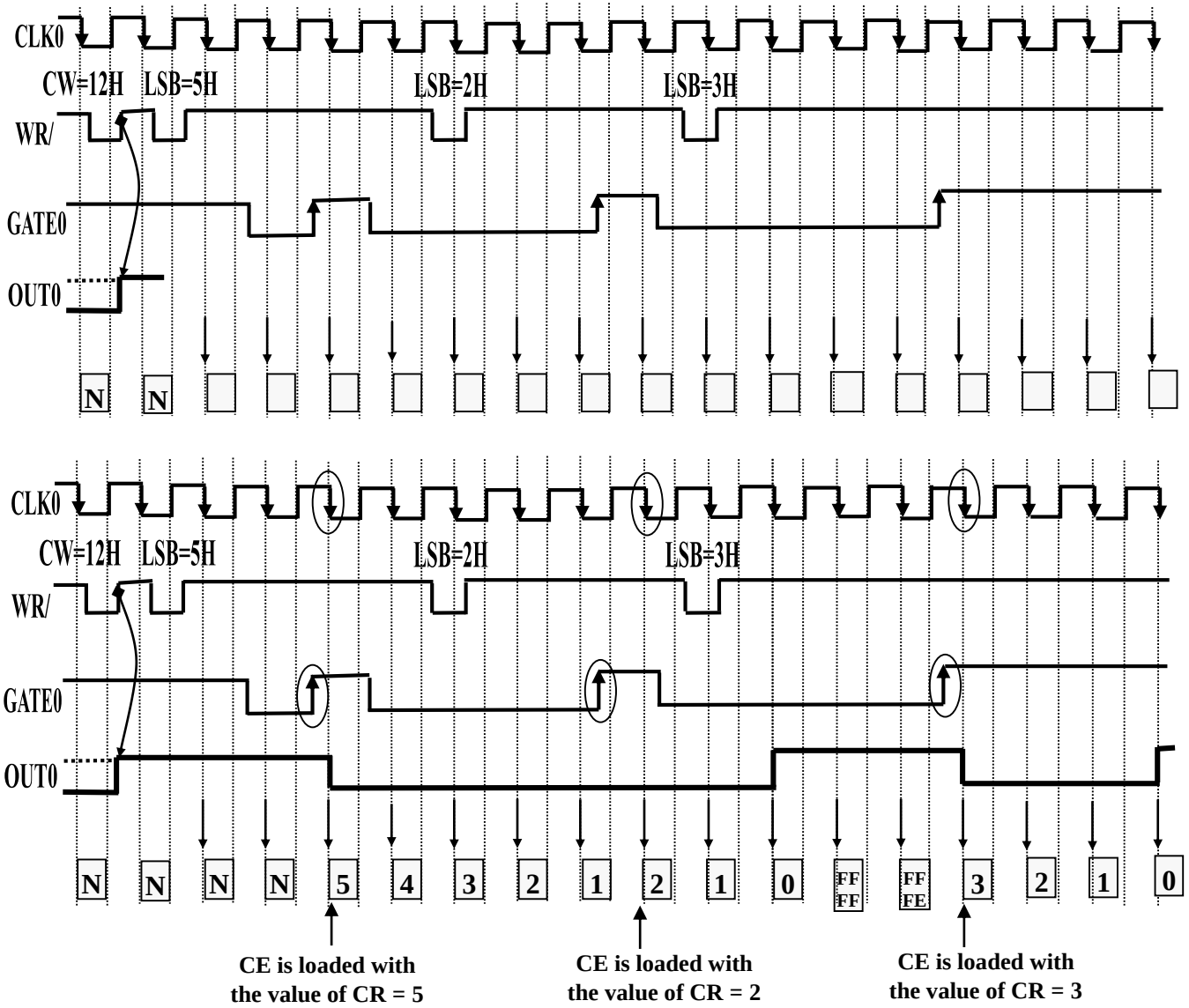
Example 2: DC Motor Speed and Direction Control - Timing



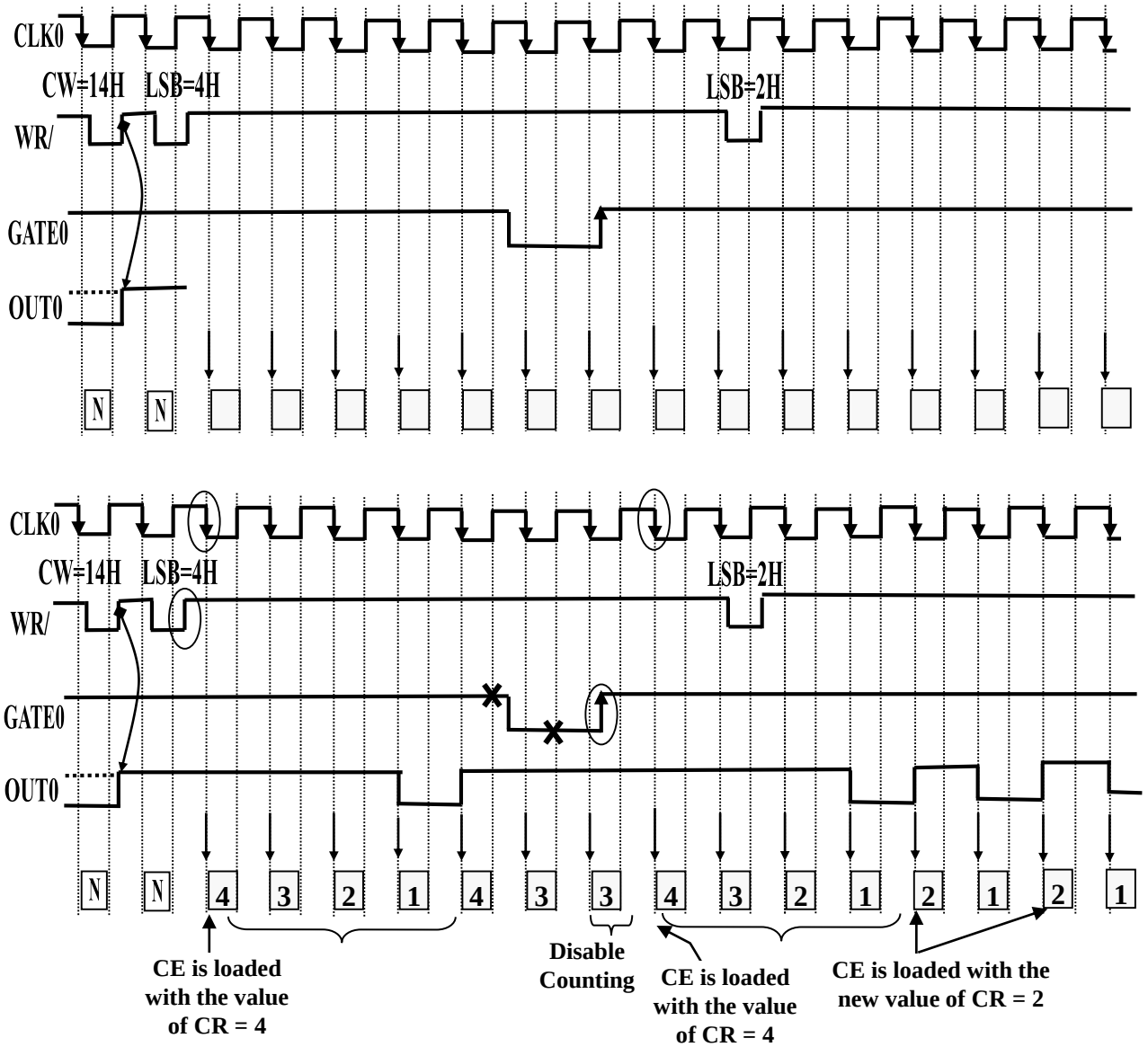
Example 3: Mode 0



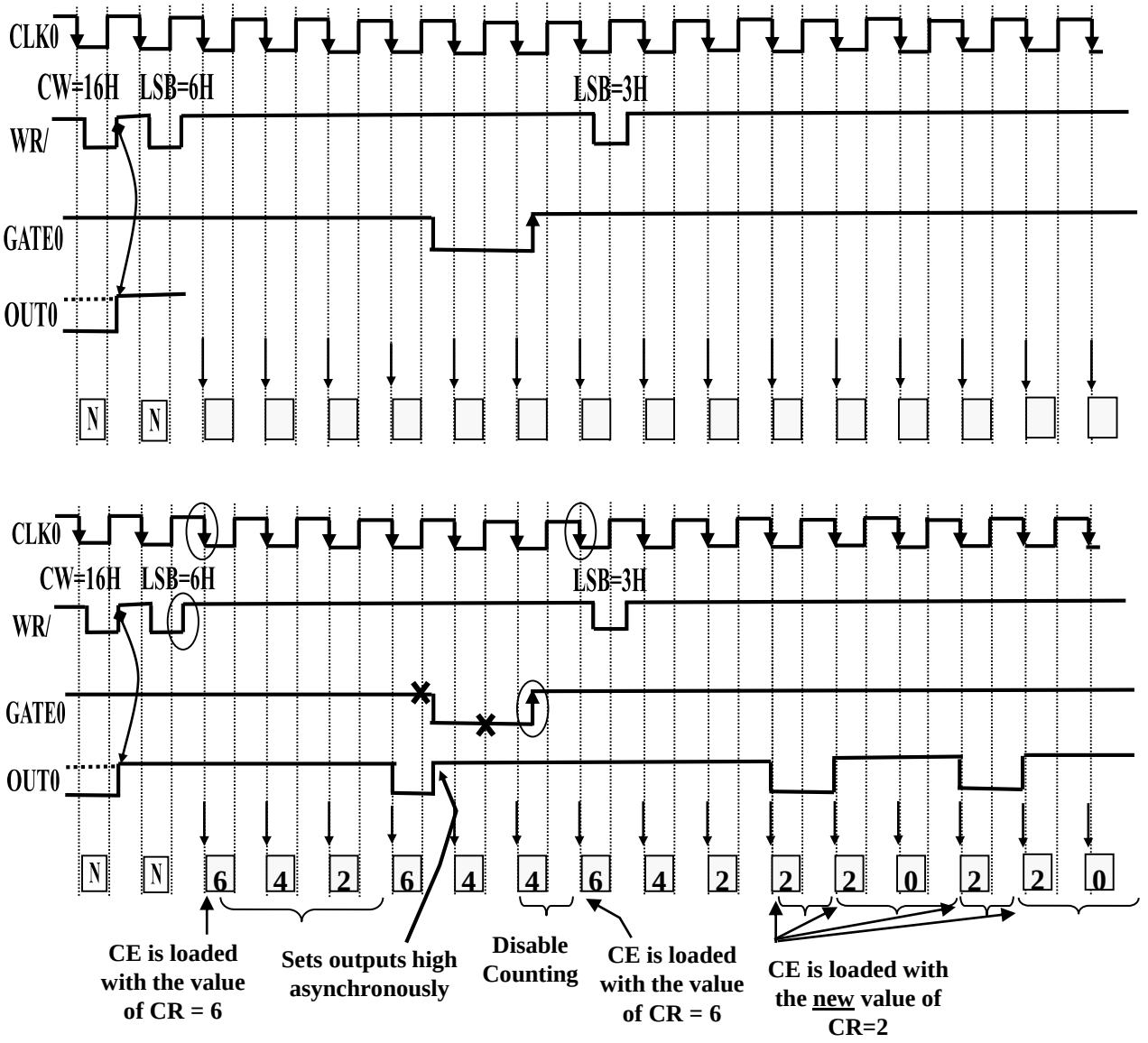
Example 4: Mode 1



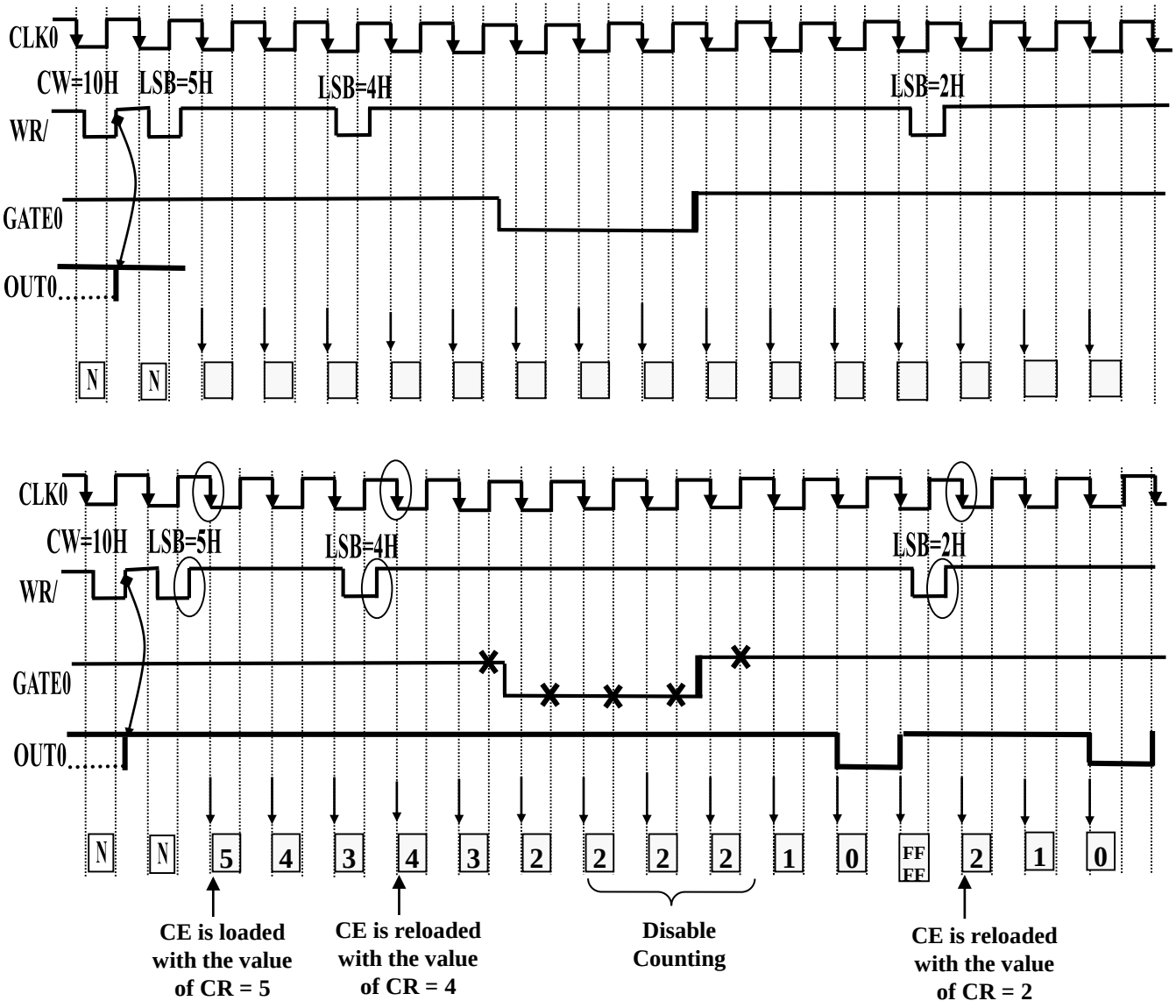
Example 5: Mode 2



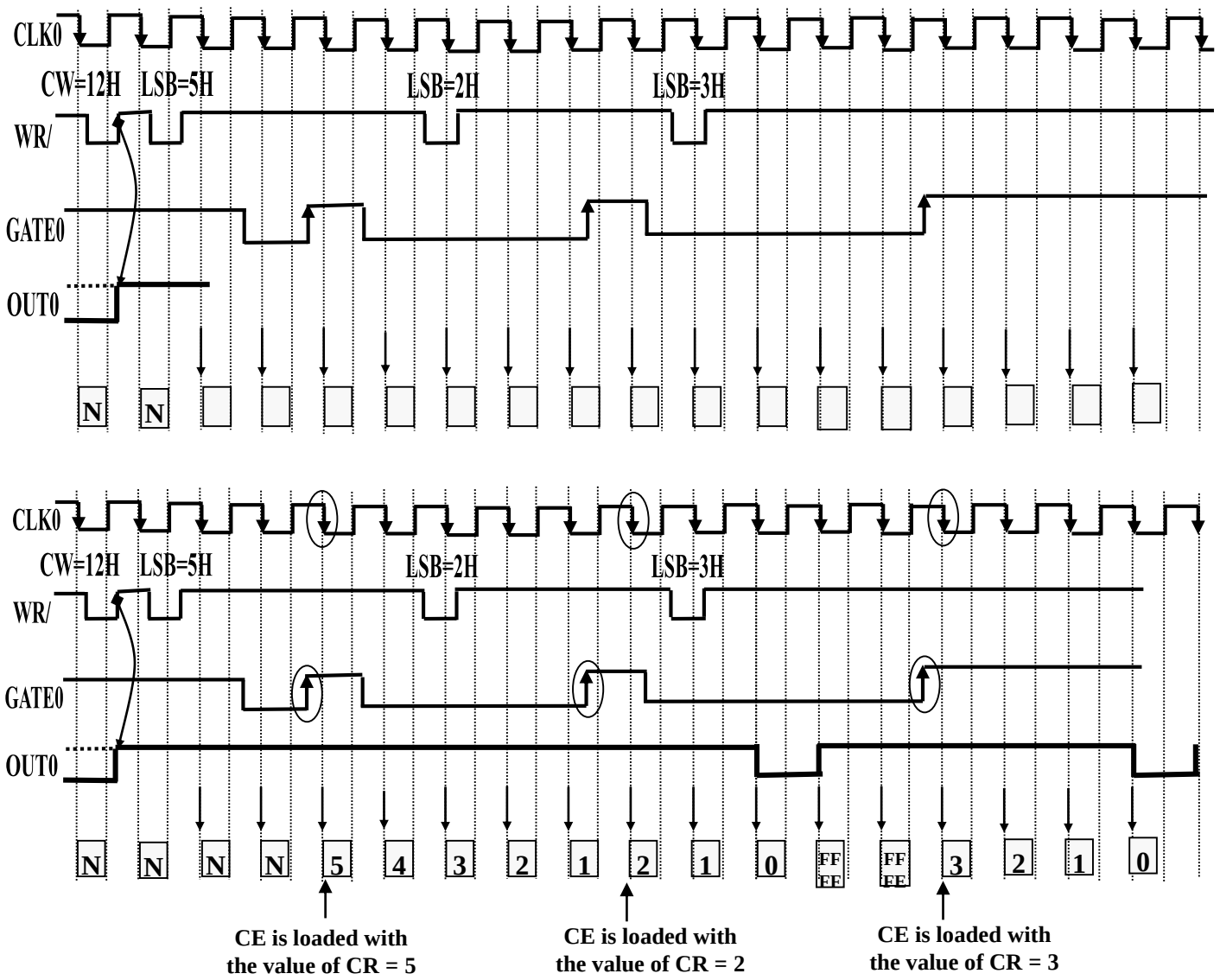
Example 6: Mode 3



Example 7: Mode 4



Example 8: Mode 5



Example 9

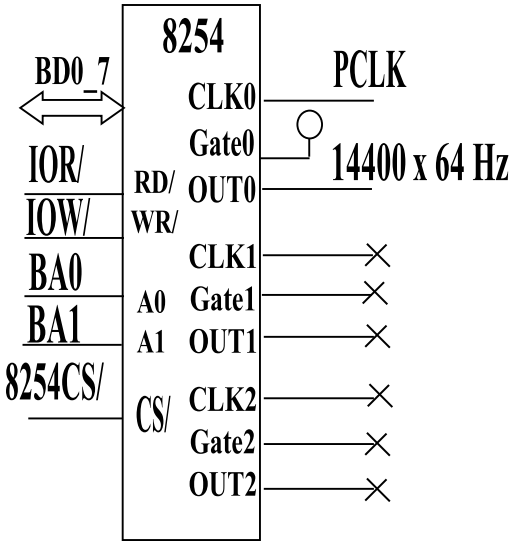
A 22.1184 MHz crystal is connected to a clock generator (8284A). The PCLK output of the 8284A is connected to the CLK0 input of 8254. You need to generate 14400 × 64 Hz square wave clock output using the counter 0 of the 8254. Write the instructions to initialize the 8254.

Solution:

C0_LSB = (22.1184×106 /6) / (14400×64)

→ **C0_LSB = 4**

```
; 8254 initialization
MOV     DX, TCW
MOV     AL, 00010110B       ; Control Word
OUT     DX, AL
;
MOV     DX, COUNTER0
MOV     AL, 4H              ;LSB
OUT     DX, AL
```



Examples

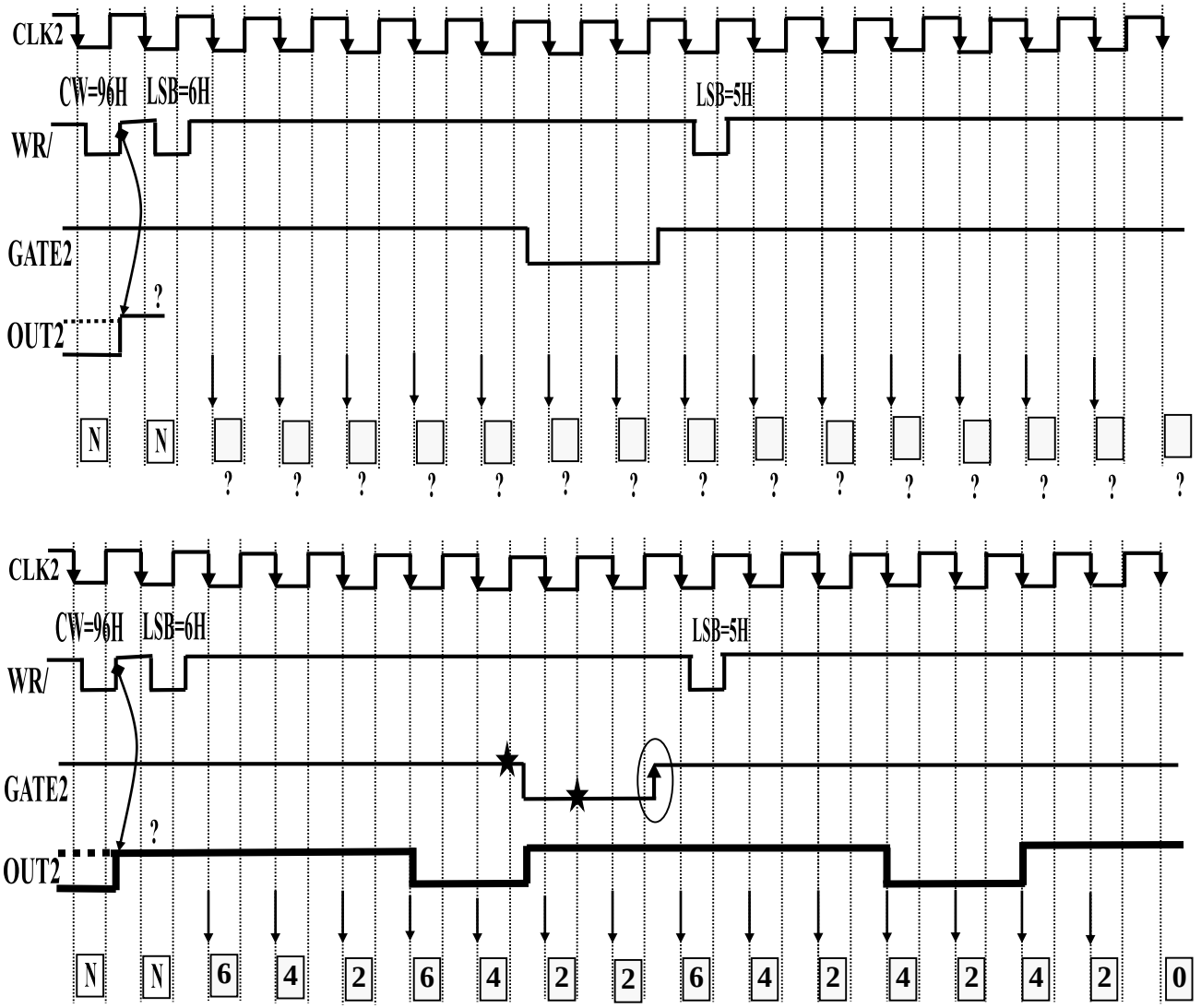
```
; Example 10: Initialize value of Counter 0 to 20d
MOV     DX, COUNTER0
MOV     AL, 20          ;LSB
OUT     DX, AL
```

```
; Example 11: Initialize value of Counter 0 to 256d
MOV     DX, COUNTER0
MOV     AL, 0           ;LSB
OUT     DX, AL
```

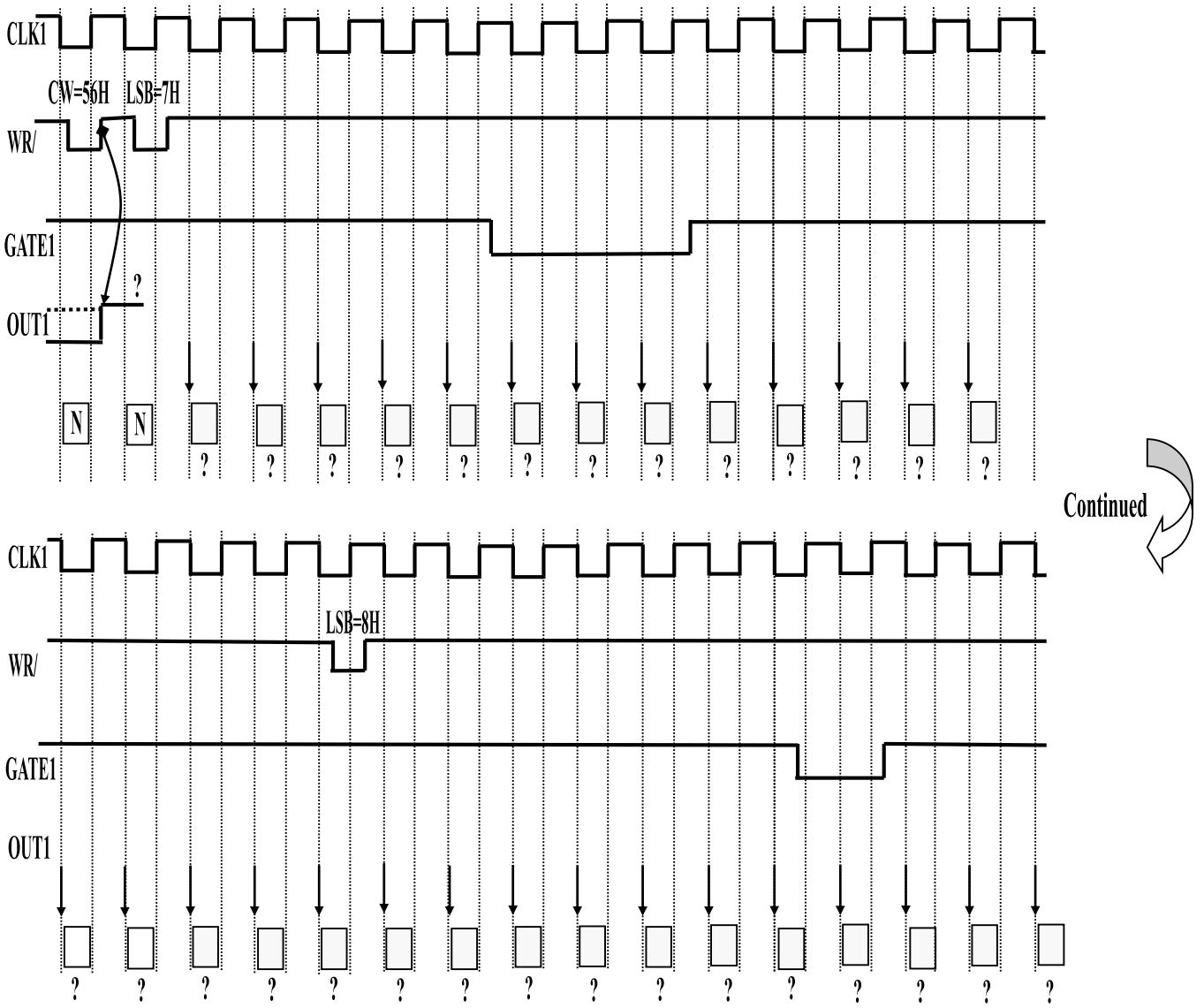
```
; Example 12: Initialize value of Counter 0 to 1000d
MOV     DX, COUNTER0
MOV     AX, 1000
OUT     DX, AL          ;LSB
MOV     AL, AH
OUT     DX, AL          ;MSB
```

```
; Example 13: Initialize value of Counter 0 to 03E8H
MOV     DX, COUNTER0
MOV     AL, 0E8H
OUT     DX, AL          ;LSB
MOV     AL, 03H
OUT     DX, AL          ;MSB
```

Example 14


CLK2
CW=96H LSB=6H
LSB=5H
WR/
GATE2
?
OUT2
N N ? ? ? ? ? ? ? ? ? ? ? ? ? ? ?
CLK2
CW=96H LSB=6H
LSB=5H
WR/
GATE2
?
OUT2
N N 6 4 2 6 4 2 2 6 4 2 4 2 4 2 0

Example 15


CLK1
CW=56H
LSB=7H
WR/
GATE1
OUT1
?
N
N
Continued
CLK1
LSB=8H
WR/
GATE1
OUT1

Solution of Example 15