# Course Specifications

| | |
|---|---|
| **Course Title:** | Digital Logic Design II |
| **Course Code:** | CENX 212 |
| **Program:** | B.S. in Computer Engineering |
| **Department:** | Department of Computer Engineering |
| **College:** | College of Computer and Information Sciences |
| **Institution:** | King Saud University |

## Table of Contents

## A. Course Identification

| |
|---|
| **1. Credit hours:** 4 (3,1,2) hours |
| **2. Course type**<br>**a.** University [ ] College [ ] Department [x] Others [ ]<br>**b.** Required [x] Elective [ ] |
| **3. Level/year at which this course is offered:** Level 5 |
| **4. Pre-requisites for this course** (if any)**:**<br>Digital Logic Design I, CENX 211 |
| **5. Co-requisites for this course** (if any)**:**<br>None |

**6. Mode of Instruction** (mark all that apply)

| No | Mode of Instruction | Contact Hours | Percentage |
|---|---|---|---|
| 1 | **Traditional classroom** | 6 hours per week | 100% |
| 2 | **Blended** | | |
| 3 | **E-learning** | | |
| 4 | **Correspondence** | | |
| 5 | **Other** | | |

**7. Actual Learning Hours** (based on academic semester)

| No | Activity | Learning Hours |
|---|---|---|
| **Contact Hours** | | |
| 1 | **Lecture** | 45 |
| 2 | **Laboratory/Studio** | 30 |
| 3 | **Tutorial** | 15 |
| 4 | **Others** (specify) | |
| | **Total** | 90 |
| **Other Learning Hours*** | | |
| 1 | **Study** | 30 |
| 2 | **Assignments** | 15 |
| 3 | **Library** | |
| 4 | **Projects/Research Essays/Theses** | |
| 5 | **Others** (specify) | |
| | **Total** | 45 |

* The length of time that a learner takes to complete learning activities that lead to achievement of course learning outcomes, such as study time, homework assignments, projects, preparing presentations, library times

## B. Course Objectives and Learning Outcomes

### 1. Course Description

Topics include: registers and counters, state machines, design of datapath and control circuits, hardware description languages (HDL) and the synthesis of logic circuits on programmable logic devices such as FPGA and CPLD

### 2. Course Main Objective

This course provides students with advanced knowledge on synchronous sequential machines and basic knowledge in programmable logic devices including hardware description language. The course includes a lab component to help students get hands-on experience with the theoretical concepts they take in the course.

### 3. Course Learning Outcomes

| CLOs | | Aligned PLOs |
|---|---|---|
| 1 | **Knowledge:** | |
| 1.1 | Explain basic memory systems and programmable logic architectures such as ROM, SRAM, DRAM, PAL, PLA, FPGA, and CPLD. | 1 |
| 1.2 | Describe the logic synthesis process that transforms an HDL description into a physical implementation. | 1 |
| 2 | **Skills:** | |
| 2.1 | Design datapath and state machine components and model them using HDL constructs. | 2 |
| 2.2 | Apply the concepts of basic timing issues, including clocking, timing constraints, and propagation delays during the design process. | 2 |
| 3 | **Competence:** | |
| 3.1 | Implement a digital system in an FPGA or CPLD and evaluate the implementation characteristics such as programmable logic resources that are used and maximum clock frequency. | 6 |

## C. Course Content

| No | List of Topics | Contact Hours |
|---|---|---|
| 1 | Registers, counters, and memory. | 8 |
| 2 | Finite state machine design. | 8 |
| 3 | Control and Datapath circuit design. | 8 |
| 4 | Propagation delays and timing constraints. | 4 |
| 5 | Programmable devices. | 8 |
| 6 | Introductory concepts in HDL. | 8 |
| 7 | Modeling and synthesis of Combinational and Sequential logic in HDL. | 12 |
| 8 | Subprograms and test benches in HDL. | 4 |
| **Total** | | 60 |

## D. Teaching and Assessment

### 1. Alignment of Course Learning Outcomes with Teaching Strategies and Assessment Methods

| Code | Course Learning Outcomes | Teaching Strategies | Assessment Methods |
|---|---|---|---|
| **1.0** | **Knowledge** | | |
| 1.1 | Discuss basic memory systems and programmable logic architectures such as ROM, SRAM, DRAM, PAL, PLA, FPGA, and CPLD. | Lecture and Tutorials | Exam / Homework |
| 1.2 | Describe the logic synthesis process that transforms an HDL description into a physical implementation. | Lecture, Tutorials, Lab demonstration | Exam / Homework |
| **2.0** | **Skills** | | |
| 2.1 | Use HDL constructs to describe combinational and sequential components in typical datapath designs. | Lecture, Tutorials, Lab demonstration | Exam / Homework |
| 2.2 | Apply the concepts of basic timing issues, including clocking, timing constraints, and propagation delays during the design process. | Lecture, Tutorials, Lab demonstration | Exam / Homework |
| **3.0** | **Competence** | | |
| 3.1 | Implement a digital system in an FPGA or CPLD and evaluate the implementation characteristics such as programmable logic resources that are used and maximum clock frequency. | Lecture, Tutorials, Lab demonstration | Exam / Homework |

### 2. Assessment Tasks for Students

| # | Assessment task* | Week Due | Percentage of Total Assessment Score |
|---|---|---|---|
| **1** | Midterm Examination (1) | 6 | 15% |
| **2** | Midterm Examination (2) | 12 | 15% |
| **3** | Homework Assignments | Weekly | 10% |
| **4** | LAB experiment | Bi-Weekly | 20% |
| **5** | Final Exam (Laboratory + Theory) | End | 40% (5+35)% |

***Assessment task** (i.e., written test, oral test, oral presentation, group project, essay, etc.)

## E. Student Academic Counseling and Support

**Arrangements for availability of faculty and teaching staff for individual student consultations and academic advice:**

1. Instructor provides at least 6 office hours per week.
2. Email consultation is available.

## F. Learning Resources and Facilities

## 1.Learning Resources

| | |
|---|---|
| **Required Textbooks** | • Verilog HDL (2nd Edition), Samir Palnitkar, Prentice Hall.<br>• Logic and Computer Design Fundamentals (4th Edition), M. Morris Mano and Charles R. Kime, Prentice Hall. |
| **Essential References Materials** | • Digital Design (3rd Edition), Morris Mano, Prentice Hall.<br>• Verilog by Example: A Concise Introduction for FPGA Design, Blaine Readler, Full Arc Press. |
| **Electronic Materials** | https://lms.ksu.edu.sa |
| **Other Learning Materials** | None |

## 2. Facilities Required

| Item | Resources |
|---|---|
| **Accommodation**<br>(Classrooms, laboratories, demonstration rooms/labs, etc.) | Lecture room with number of seats enough to accommodate enrolled students. |
| **Technology Resources**<br>(AV, data show, Smart Board, software, etc.) | Overhead projector with required software to facilitate presentations on smart board. |
| **Other Resources**<br>(Specify, e.g. if specific laboratory equipment is required, list requirements or attach a list) | NO |

# G. Course Quality Evaluation

| Evaluation Areas/Issues | Evaluators | Evaluation Methods |
|---|---|---|
| Extent of achievement of course learning outcomes | Faculty | Attainment level of every CLO is measured directly. |
| Extent of achievement of course learning outcomes | Students | Attainment level of every CLO is measured indirectly. |
| Quality of learning resources | Students | Indirect – Edugate survey. |
| Effectiveness of assessment | Faculty-Peer Review | Final examination is moderated. |
| Effectiveness of teaching and assessment | Department Council | Course reports are evaluated by the Department Council. |

**Evaluation areas** (e.g., Effectiveness of teaching and assessment, Extent of achievement of course learning outcomes, Quality of learning resources, etc.)
**Evaluators** (Students, Faculty, Program Leaders, Peer Reviewer, Others (specify)
**Assessment Methods** (Direct, Indirect)

# H. Specification Approval Data

| | |
|---|---|
| **Council / Committee** | |
| **Reference No.** | |
| **Date** | |