Question 1:

a) Design a 14/1 line multiplexer using 8/1 line multiplexers. Use only multiplexer chips.

(3 Marks)

b) Implement the following function using only one 4/1 multiplexer chip.

$F(x, y, z) = \Sigma (1, 2, 3, 7)$

(4 Marks)

Answer to question 1:

Question 2:

a) Compute the ROM size to implement the following functions

$F_1(a, b, c, d) = \Sigma\ (4,5,14,15)$

$F_2(a, b, c) = \Sigma\ (1,3,4,6)$

(3 Marks)

b) Draw the internal ROM connections to implement the above functions in part (a)

(4 Marks)

Answer to question 2:

Question 3:

a) Design a hardware to generate the 2's complement for a 3-bit binary code (X_2 X_1 X_0) using only half adder blocks

(3 Marks)

b) Design a digital comparator to compare between two input codes (X & Y). Each code consists of two binary bits. The output of the circuit will be one if the two codes are equal (i.e $X_1X_0 = Y_1Y_0$).
(*hint*: use a decoder with inverted outputs)

(4 Marks)

Answer to question 3: